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ILI9340

a-Si TFT LCD Single Chip Driver
240RGBx320 Resolution and 262K color

Specification
Preliminary

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1. Introduction

ILI9340 is a 262,144-color single-chip SOC driver for a-TFT liquid crystal display with resolution of 240RGBx320 dots, comprising a 720-channel source driver, a 320-channel gate driver, 172,800 bytes GRAM for graphic display data of 240RGBx320 dots, and power supply circuit.

ILI9340 supports parallel 8-/9-/16-/18-bit data bus MCU interface, 8-/16-/18-bit data bus RGB interface and 3-/4-line serial peripheral interface (SPI). The moving picture area can be specified in internal GRAM by window address function. The specified window area can be updated selectively, so that moving picture can be displayed simultaneously independent of still picture area.

ILI9340 can operate with 1.65V ~ 3.3V I/O interface voltage and an incorporated voltage follower circuit to generate voltage levels for driving an LCD. ILI9340 supports full color, 8-color display mode and sleep mode for precise power control by software and these features make the ILI9340 an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, MP3 and PMP where long battery life is a major concern.

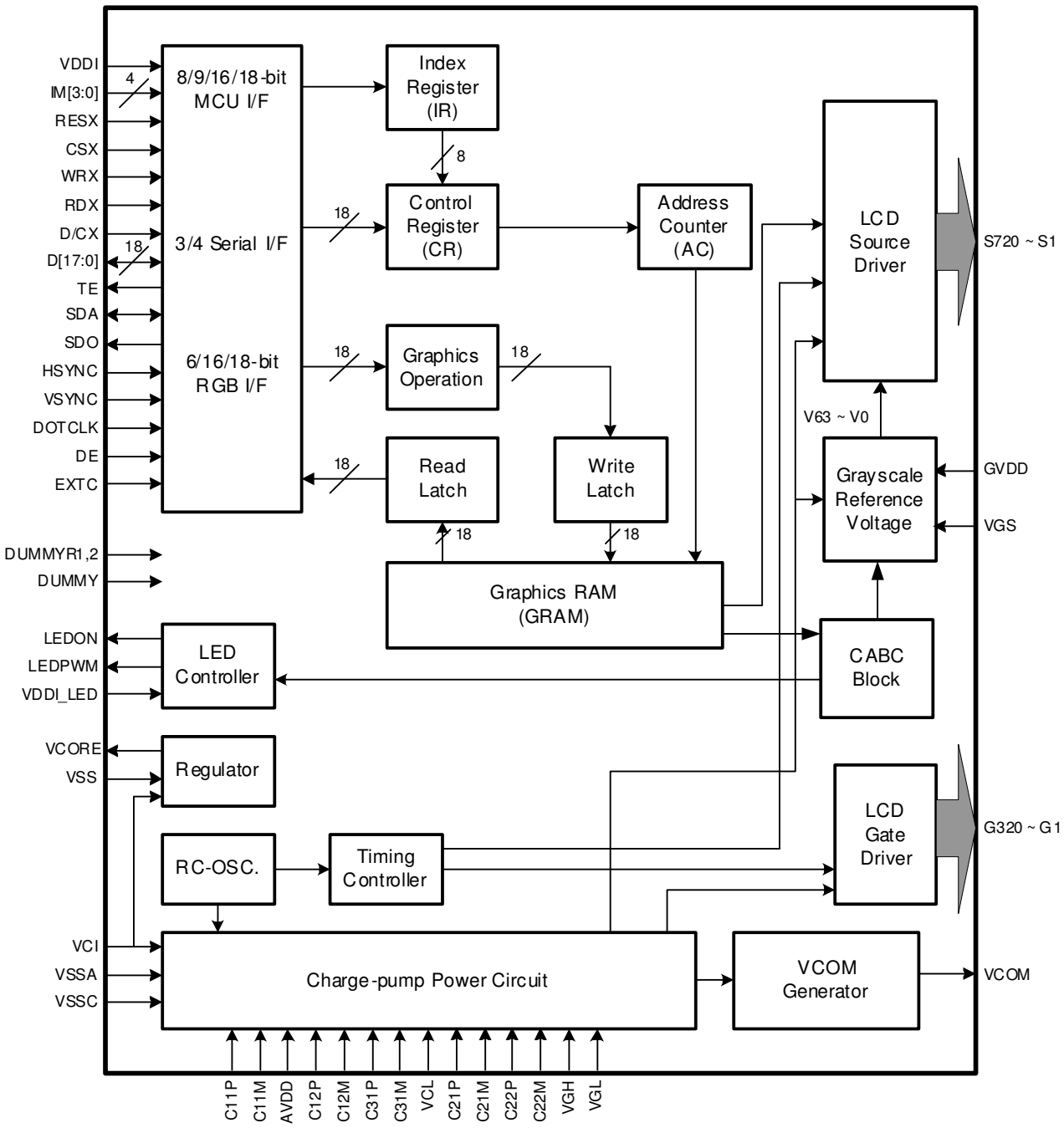
2. Features

- Display resolution: [240xRGB](H) x 320(V)
- Output:
  - 720 source outputs
  - 320 gate outputs
  - Common electrode output (VCOM)
- a-TFT LCD driver with on-chip full display RAM: 172,800 bytes
- System Interface
  - 8-bits, 9-bits, 16-bits, 18-bits interface with 8080-Ⅰ/8080-Ⅱ series MCU
  - 6-bits, 16-bits, 18-bits RGB interface with graphic controller
  - 3-line / 4-line serial interface
- Display mode:
  - Full color mode (Idle mode OFF): 262K-color (selectable color depth mode by software)
  - Reduce color mode (Idle mode ON): 8-color
- Power saving mode:
  - Sleep mode
- On chip functions:
  - VCOM generator and adjustment
  - Timing generator
  - Oscillator
  - DC/DC converter
  - Line/frame inversion
  - 4 preset Gamma curves with separate RGB Gamma correction
- Dynamic backlight control
- MTP (3 times):
  - 8-bits for ID1, ID2, ID3
  - 7-bits for VCOM adjustment
- Low -power consumption architecture

- Low operating power supplies:
  - VDDI = 1.65V ~ 3.3V (logic)
  - VCI = 2.5V ~ 3.3V (analog)

- LCD Voltage drive:
  - Source/VCOM power supply voltage
    - AVDD - GND = 4.5V ~ 6.0V
    - VCL - GND = -2.0V ~ -3.0V
    - VCI1 - VCL ≦ 6.0V
  - Gate driver output voltage
    - VGH - GND = 10.0V ~ 20.0V
    - VGL - GND = -5.0V ~ -15.0V
    - VGH - VGL ≦ 32V
  - VCOM driver output voltage
    - VCOMH = 3.0V ~ (AVDD – 0.5)V
    - VCOML = (VCL+0.5)V ~ 0V
    - VCOMH - VCOML ≦ 6.0V
- Operate temperature range: -40℃ to 80℃
- a-Si TFT LCD storage capacitor : Cst on Common structure only

3. Block Diagram



4. Pin Descriptions

Power Supply Pins			
Pin Name	**I/O**	**Type**	**Descriptions**
VDDI	I	P	Low voltage power supply for interface logic circuits (1.65 ~ 3.3 V)
VDDI_LED	I		Power supply for LED driver interface. (1.65 ~ 3.3 V) If LED driver is not used, fix this pin at VDDI.
VCI	I	Analog Power	High voltage power supply for analog circuit blocks (2.5 ~ 3.3 V)
Vcore	I	Digital Power	Regulated Low voltage level for interface circuits Connect a capacitor for stabilization. Don't apply any external power to this pad
VSS3	I	I/O Ground	System ground level for I/O circuits.
VSS	I	Digital Ground	System ground level for logic blocks
VSSA	I	Analog Ground	System ground level for analog circuit blocks Connect to VSS on the FPC to prevent noise.
VSSC	I	Analog Ground	System ground level for analog circuit blocks Connect to VSS on the FPC to prevent noise

<table>
<tr><th colspan="3">Interface Logic Signals</th></tr>
<tr><th>Pin Name</th><th>I/O</th><th>Type</th><th>Descriptions</th></tr>
<tr><td>IM[3:0]</td><td>I</td><td>(VDDI/VSS)</td><td>- Select the MCU interface mode
<table>
<tr><th rowspan="2">IM3</th><th rowspan="2">IM2</th><th rowspan="2">IM1</th><th rowspan="2">IM0</th><th rowspan="2">MCU-Interface Mode</th><th colspan="2">DB Pin in use</th></tr>
<tr><th>Register/Content</th><th>GRAM</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>80 MCU 8-bit bus interface Ⅰ</td><td>D[7:0]</td><td>D[7:0]</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>80 MCU 16-bit bus interface Ⅰ</td><td>D[7:0]</td><td>D[15:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>80 MCU 9-bit bus interface Ⅰ</td><td>D[7:0]</td><td>D[8:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>80 MCU 18-bit bus interface Ⅰ</td><td>D[7:0]</td><td>D[17:0]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>3-wire 9-bit data serial interface Ⅰ</td><td colspan="2">SDA: In/OUT</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>4-wire 8-bit data serial interface Ⅰ</td><td colspan="2">SDA: In/OUT</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>80 MCU 16-bit bus interface Ⅱ</td><td>D[8:1]</td><td>D[17:10]
D[8:1]</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>80 MCU 8-bit bus interface Ⅱ</td><td>D[17:10]</td><td>D[17:10],</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>80 MCU 18-bit bus interface Ⅱ</td><td>D[8:1]</td><td>D[17:0]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>80 MCU 9-bit bus interface Ⅱ</td><td>D[17:10]</td><td>D[17:9]</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>3-wire 9-bit data serial interface Ⅱ</td><td colspan="2">SDI: In
SDO: Out</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>4-wire 8-bit data serial interface Ⅱ</td><td colspan="2">SDI: In
SDO: Out</td></tr>
</table>
MPU Parallel interface bus and serial interface select
If use RGB Interface must select serial interface.
* : Fix this pin at VDDI or VSS.</td></tr>
<tr><td>RESX</td><td>I</td><td>MCU
(VDDI/VSS)</td><td>This signal will reset the device and must be applied to properly initialize the chip.
Signal is active low.</td></tr>
<tr><td>EXTC</td><td>I</td><td>MCU
(VDDI/VSS)</td><td>Extended command set enable.
Low: extended command set is discarded.
High: extended command set is accepted.

Please connect EXTC to VDDI to read/write extended registers (RB0h~RCFh, RE0h~RFFh)</td></tr>
<tr><td>CSX</td><td>I</td><td>MCU
(VDDI/VSS)</td><td>Chip select input pin (“Low” enable).
This pin can be permanently fixed “Low” in MPU interface mode only.
* note1,2</td></tr>
<tr><td>D/CX (SCL)</td><td>I</td><td>MCU
(VDDI/VSS)</td><td>This pin is used to select “Data or Command” in the parallel interface or 4-wire 8-bit serial data interface.
When DCX = ’1’, data is selected.
When DCX = ’0’, command is selected.
This pin is used serial interface clock in 3-wire 9-bit / 4-wire 8-bit serial data interface.
If not used, this pin should be connected to VDDI or VSS.</td></tr>
</table>

RDX	I	MCU (VDDI/VSS)	8080-Ⅰ/8080-Ⅱ system (RDX): Serves as a read signal and MCU read data at the rising edge. *Fix to VDDI or VSS level when not in use.*
WRX (D/CX)	I	MCU (VDDI/VSS)	- 8080-Ⅰ/8080-Ⅱ system (WRX): Serves as a write signal and writes data at the rising edge. - 4-line system (D/CX): Serves as command or parameter select. *Fix to VDDI or VSS level when not in use.*
D[17:0]	I/O	MCU (VDDI/VSS)	18-bit parallel bi-directional data bus for MCU system and RGB interface mode *Fix to VSS level when not in use*
SDI/SDA	I/O	MCU (VDDI/VSS)	When IM[3] : Low, Serial in/out signal. When IM[3] : High, Serial input signal. The data is applied on the rising edge of the SCL signal. If not used, fix this pin at VDDI or VSS.
SDO	O	MCU (VDDI/VSS)	Serial output signal. The data is outputted on the falling edge of the SCL signal. If not used, open this pin
TE	O	MCU (VDDI/VSS)	Tearing effect output pin to synchronize MPU to frame writing, activated by S/W command. When this pin is not activated, this pin is low. If not used, open this pin.
DOTCLK	I	MCU (VDDI/VSS)	Dot clock signal for RGB interface operation. *Fix to VDDI or VSS level when not in use.*
VSYNC	I	MCU (VDDI/VSS)	Frame synchronizing signal for RGB interface operation. *Fix to VDDI or VSS level when not in use.*
HSYNC	I	MCU (VDDI/VSS)	Line synchronizing signal for RGB interface operation. *Fix to VDDI or VSS level when not in use.*
DE	I	MCU (VDDI/VSS)	Data enable signal for RGB interface operation. *Fix to VDDI or VSS level when not in use.*

Note.

1. If CSX is connected to VSS in Parallel interface mode, there will be no abnormal visible effect to the display module. Also there will be no restriction on using the Parallel Read/Write protocols, Power On/Off Sequences or other functions. Furthermore there will be no influence to the Power Consumption of the display module.

2. When CSX=’1’, there is no influence to the parallel and serial interface.

LCD Driver Input/Output Pins			
Pin Name	**I/O**	**Type**	**Descriptions**
S720~S1	O	Source	Source output signals.. *Leave the pin to open when not in use.*
G320~G1	O	Gate	Gate output signals. *Leave the pin to open when not in use.*
VCI1	O	Power	An internal reference voltage generated between VCI and VSSA. Reference input voltage for 1st and 3rd step up circuit.
AVDD	O	Power	Output voltage of 1st step up circuit (2 x VCI1). Input voltage to 2nd step up circuit. Generated power output pad for source driver block. Connect this pad to the capacitor for stabilization.
VGH	O	Power	Power supply for the gate driver. Adjust the VGH level with the BT[3:0] bits. Connect this pad with a stabilizing capacitor.
VGL	O	Power	Power supply for the gate driver. Adjust the VGL level with the BT[3:0] bits. Connect this pad with a stabilizing capacitor.
VCL	P	Stabilizing capacitor	Power supply for VCOML. VCL = 0~ - VCI1 Connect this pad with a stabilizing capacitor.
C11P, C11M C12P, C12M	P		Connect the charge-pumping capacitor for generating AVDD level.
C21P, C21M C22P, C22M	P		Connect the charge-pumping capacitor for generating VGH, VGL level.
C31P, C31M	P		Connect the charge-pumping capacitor for generating VCL level.
GVDD	O		High reference voltage for grayscale voltage generator. Internal register can be used to adjust the voltage.
VGS	I		Low reference voltage for grayscale voltage generator. Connect an external resistor or to system ground.
VCOM	O		Power supply pad for the TFT- display counter electrode. Charge recycling method is used with VCI and VSSA voltage. Connect this pad to the TFT-display counter electrode.
LEDPWM	O		Output pin for PWM (Pulse Width Modulation) signal of LED driving. If not used, open this pad.
LEDON	O		Output pin for enabling LED driving. If not used, open this pad.

Test Pins			
Pin Name	**I/O**	**Type**	**Descriptions**
DUMMYR1 DUMMYR2	I		Contact resistance measurement pad. In normal operation, leave this unconnected. These pads are at VSS level. When measuring an ohmic resistance of the contact, do not apply any power.
DUMMY	-	Open	Input pads used only for test purpose at IC-side. During normal operation, leave these pads open.

Liquid crystal power supply specifications Table

No.	Item		Description
1	TFT Source Driver		720 pins (240 x RGB)
2	TFT Gate Driver		320 pins
3	TFT Display's Capacitor Structure		Cst structure only (Cs on Common)
4	Liquid Crystal Drive Output	S1 ~ S720	V0 ~ V63 grayscales
		G1 ~ G320	VGH - VGL
		VCOM	VCOMH - VCOML: Amplitude = electronic volumes
5	Input Voltage	VDDI	1.65V ~ 3.30V
		VCI	2.50V ~ 3.30V
6	Liquid Crystal Drive Voltages	AVDD	4.5V ~ 6.0V
		VGH	10.0V ~ 20.0V
		VGL	-5.0V ~ -15.0V
		VCL	-1.9V ~ -3.0V
		VGH - VGL	Max. 32.0V
		VCI1 - VCL	Max. 6.0V
7	Internal Step-up Circuits	AVDD	VCI1 x2, x3
		VGH	VCI1 x4, x5, x6, x7, x9
		VGL	VCI1 x-3, x-4, x-5, x-6, x-7
		VCL	VCI1 x-1

Note: VCI1 is an internal reference voltage for the step-up circuit1.

5. Pad Arrangement and Coordination

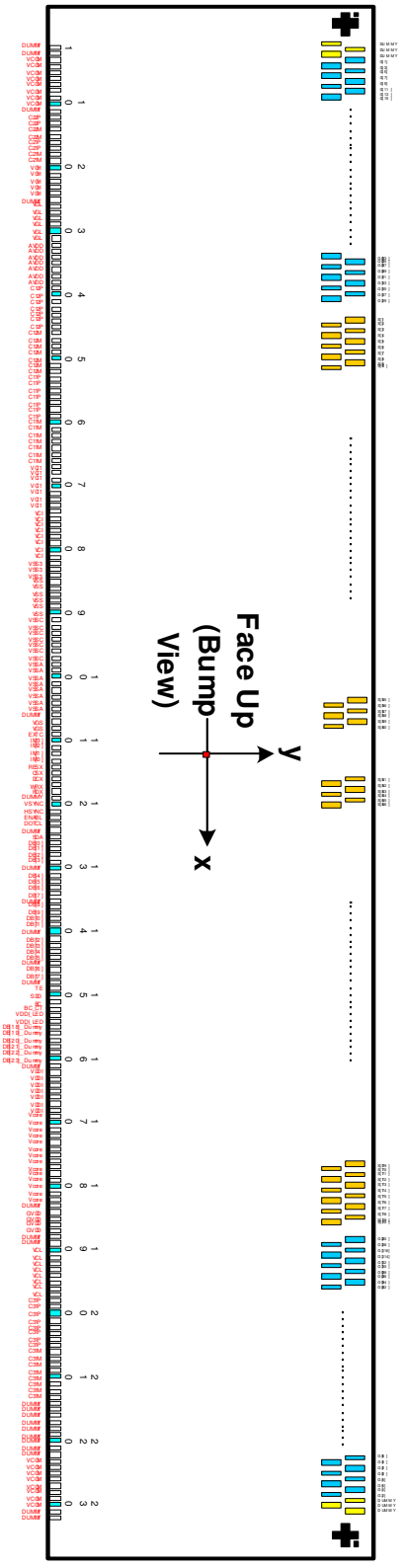
Chip Size: 16200um x 728um

Chip thickness :280um (typ.)

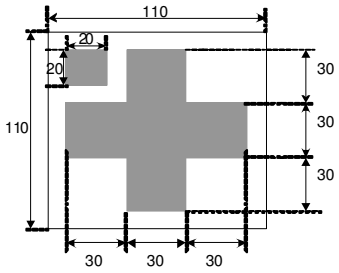
Pad Location: Pad Center.

Coordinate Origin: Chip center

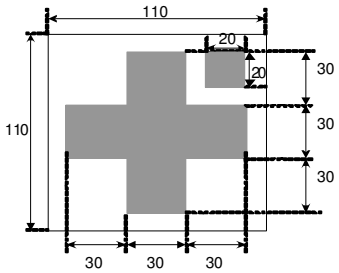
Au bump height: 12um (typ.)



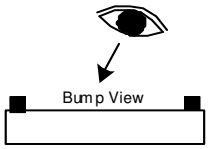
Alignment Marks



Alignment Mark: A1



Alignment Mark: A2



No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
1	DUMMY	-7292.5	-285	51	C12M	-4292.5	-285	101	VSSA	-1292.5	-285	151	LEDPWM	2245	-285
2	DUMMY	-7232.5	-285	52	C12M	-4232.5	-285	102	VSSA	-1232.5	-285	152	LEDON	2330	-285
3	VCOM	-7172.5	-285	53	C11P	-4172.5	-285	103	VSSA	-1172.5	-285	153	VDDI_LED	2402.5	-285
4	VCOM	-7112.5	-285	54	C11P	-4112.5	-285	104	VSSA	-1112.5	-285	154	VDDI_LED	2462.5	-285
5	VCOM	-7052.5	-285	55	C11P	-4052.5	-285	105	VSSA	-1052.5	-285	155	DB[18]_Dummy	2535	-285
6	VCOM	-6992.5	-285	56	C11P	-3992.5	-285	106	DUMMY	-992.5	-285	156	DB[19]_Dummy	2620	-285
7	VCOM	-6932.5	-285	57	C11P	-3932.5	-285	107	VGS	-932.5	-285	157	DB[20]_Dummy	2705	-285
8	VCOM	-6872.5	-285	58	C11P	-3872.5	-285	108	VGS	-872.5	-285	158	DB[21]_Dummy	2790	-285
9	VCOM	-6812.5	-285	59	C11P	-3812.5	-285	109	EXTC	-812.5	-285	159	DB[22]_Dummy	2875	-285
10	VCOM	-6752.5	-285	60	C11M	-3752.5	-285	110	IM<3>	-752.5	-285	160	DB[23]_Dummy	2960	-285
11	DUMMY	-6692.5	-285	61	C11M	-3692.5	-285	111	IM<2>	-692.5	-285	161	DUMMY	3032.5	-285
12	C22P	-6632.5	-285	62	C11M	-3632.5	-285	112	IM<1>	-632.5	-285	162	VDDI	3092.5	-285
13	C22P	-6572.5	-285	63	C11M	-3572.5	-285	113	IM<0>	-572.5	-285	163	VDDI	3152.5	-285
14	C22M	-6512.5	-285	64	C11M	-3512.5	-285	114	RESX	-512.5	-285	164	VDDI	3212.5	-285
15	C22M	-6452.5	-285	65	C11M	-3452.5	-285	115	CSX	-452.5	-285	165	VDDI	3272.5	-285
16	C21P	-6392.5	-285	66	C11M	-3392.5	-285	116	DCX	-392.5	-285	166	VDDI	3332.5	-285
17	C21P	-6332.5	-285	67	VCI1	-3332.5	-285	117	WRX	-332.5	-285	167	VDDI	3392.5	-285
18	C21M	-6272.5	-285	68	VCI1	-3272.5	-285	118	RDX	-272.5	-285	168	VDDI	3452.5	-285
19	C21M	-6212.5	-285	69	VCI1	-3212.5	-285	119	DUMMY	-212.5	-285	169	Vcore	3512.5	-285
20	VGH	-6152.5	-285	70	VCI1	-3152.5	-285	120	VSYNC	-152.5	-285	170	Vcore	3572.5	-285
21	VGH	-6092.5	-285	71	VCI1	-3092.5	-285	121	HSYNC	-92.5	-285	171	Vcore	3632.5	-285
22	VGH	-6032.5	-285	72	VCI1	-3032.5	-285	122	ENABL	-32.5	-285	172	Vcore	3692.5	-285
23	VGH	-5972.5	-285	73	VCI1	-2972.5	-285	123	DOTCLK	27.5	-285	173	Vcore	3752.5	-285
24	VGH	-5912.5	-285	74	VCI	-2912.5	-285	124	DUMMY	87.5	-285	174	Vcore	3812.5	-285
25	DUMMY	-5852.5	-285	75	VCI	-2852.5	-285	125	SDA	160	-285	175	Vcore	3872.5	-285
26	VGL	-5792.5	-285	76	VCI	-2792.5	-285	126	DB[0]	245	-285	176	Vcore	3932.5	-285
27	VGL	-5732.5	-285	77	VCI	-2732.5	-285	127	DB[1]	330	-285	177	Vcore	3992.5	-285
28	VGL	-5672.5	-285	78	VCI	-2672.5	-285	128	DB[2]	415	-285	178	Vcore	4052.5	-285
29	VGL	-5612.5	-285	79	VCI	-2612.5	-285	129	DB[3]	500	-285	179	Vcore	4112.5	-285
30	VGL	-5552.5	-285	80	VCI	-2552.5	-285	130	DUMMY	572.5	-285	180	Vcore	4172.5	-285
31	VGL	-5492.5	-285	81	VCI	-2492.5	-285	131	DB[4]	645	-285	181	Vcore	4232.5	-285
32	AVDD	-5432.5	-285	82	VSS3	-2432.5	-285	132	DB[5]	730	-285	182	Vcore	4292.5	-285
33	AVDD	-5372.5	-285	83	VSS3	-2372.5	-285	133	DB[6]	815	-285	183	DUMMY	4352.5	-285
34	AVDD	-5312.5	-285	84	VSS3	-2312.5	-285	134	DB[7]	900	-285	184	GVDD	4412.5	-285
35	AVDD	-5252.5	-285	85	VSS	-2252.5	-285	135	DUMMY	972.5	-285	185	GVDD	4472.5	-285
36	AVDD	-5192.5	-285	86	VSS	-2192.5	-285	136	DB[8]	1045	-285	186	GVDD	4532.5	-285
37	AVDD	-5132.5	-285	87	VSS	-2132.5	-285	137	DB[9]	1130	-285	187	GVDD	4592.5	-285
38	AVDD	-5072.5	-285	88	VSS	-2072.5	-285	138	DB[10]	1215	-285	188	DUMMY	4652.5	-285
39	C12P	-5012.5	-285	89	VSS	-2012.5	-285	139	DB[11]	1300	-285	189	DUMMY	4712.5	-285
40	C12P	-4952.5	-285	90	VSS	-1952.5	-285	140	DUMMY	1372.5	-285	190	VCL	4772.5	-285
41	C12P	-4892.5	-285	91	VSSC	-1892.5	-285	141	DB[12]	1445	-285	191	VCL	4832.5	-285
42	C12P	-4832.5	-285	92	VSSC	-1832.5	-285	142	DB[13]	1530	-285	192	VCL	4892.5	-285
43	C12P	-4772.5	-285	93	VSSC	-1772.5	-285	143	DB[14]	1615	-285	193	VCL	4952.5	-285
44	C12P	-4712.5	-285	94	VSSC	-1712.5	-285	144	DB[15]	1700	-285	194	VCL	5012.5	-285
45	C12P	-4652.5	-285	95	VSSC	-1652.5	-285	145	DUMMY	1772.5	-285	195	VCL	5072.5	-285
46	C12M	-4592.5	-285	96	VSSC	-1592.5	-285	146	DB[16]	1845	-285	196	VCL	5132.5	-285
47	C12M	-4532.5	-285	97	VSSC	-1532.5	-285	147	DB[17]	1930	-285	197	VCL	5192.5	-285
48	C12M	-4472.5	-285	98	VSSA	-1472.5	-285	148	DUMMY	2002.5	-285	198	C31P	5252.5	-285
49	C12M	-4412.5	-285	99	VSSA	-1412.5	-285	149	TE	2075	-285	199	C31P	5312.5	-285
50	C12M	-4352.5	-285	100	VSSA	-1352.5	-285	150	SDO	2160	-285	200	C31P	5372.5	-285

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
201	C31P	5432.5	-285	251	G32	7147	261	301	G132	6447	261	351	G232	5747	261
202	C31P	5492.5	-285	252	G34	7133	126	302	G134	6433	126	352	G234	5733	126
203	C31P	5552.5	-285	253	G36	7119	261	303	G136	6419	261	353	G236	5719	261
204	C31P	5612.5	-285	254	G38	7105	126	304	G138	6405	126	354	G238	5705	126
205	C31P	5672.5	-285	255	G40	7091	261	305	G140	6391	261	355	G240	5691	261
206	C31M	5732.5	-285	256	G42	7077	126	306	G142	6377	126	356	G242	5677	126
207	C31M	5792.5	-285	257	G44	7063	261	307	G144	6363	261	357	G244	5663	261
208	C31M	5852.5	-285	258	G46	7049	126	308	G146	6349	126	358	G246	5649	126
209	C31M	5912.5	-285	259	G48	7035	261	309	G148	6335	261	359	G248	5635	261
210	C31M	5972.5	-285	260	G50	7021	126	310	G150	6321	126	360	G250	5621	126
211	C31M	6032.5	-285	261	G52	7007	261	311	G152	6307	261	361	G252	5607	261
212	C31M	6092.5	-285	262	G54	6993	126	312	G154	6293	126	362	G254	5593	126
213	C31M	6152.5	-285	263	G56	6979	261	313	G156	6279	261	363	G256	5579	261
214	DUMMYR1	6212.5	-285	264	G58	6965	126	314	G158	6265	126	364	G258	5565	126
215	DUMMYR2	6272.5	-285	265	G60	6951	261	315	G160	6251	261	365	G260	5551	261
216	DUMMY	6332.5	-285	266	G62	6937	126	316	G162	6237	126	366	G262	5537	126
217	DUMMY	6392.5	-285	267	G64	6923	261	317	G164	6223	261	367	G264	5523	261
218	DUMMY	6452.5	-285	268	G66	6909	126	318	G166	6209	126	368	G266	5509	126
219	DUMMY	6512.5	-285	269	G68	6895	261	319	G168	6195	261	369	G268	5495	261
220	DUMMY	6572.5	-285	270	G70	6881	126	320	G170	6181	126	370	G270	5481	126
221	DUMMY	6632.5	-285	271	G72	6867	261	321	G172	6167	261	371	G272	5467	261
222	DUMMY	6692.5	-285	272	G74	6853	126	322	G174	6153	126	372	G274	5453	126
223	VCOM	6752.5	-285	273	G76	6839	261	323	G176	6139	261	373	G276	5439	261
224	VCOM	6812.5	-285	274	G78	6825	126	324	G178	6125	126	374	G278	5425	126
225	VCOM	6872.5	-285	275	G80	6811	261	325	G180	6111	261	375	G280	5411	261
226	VCOM	6932.5	-285	276	G82	6797	126	326	G182	6097	126	376	G282	5397	126
227	VCOM	6992.5	-285	277	G84	6783	261	327	G184	6083	261	377	G284	5383	261
228	VCOM	7052.5	-285	278	G86	6769	126	328	G186	6069	126	378	G286	5369	126
229	VCOM	7112.5	-285	279	G88	6755	261	329	G188	6055	261	379	G288	5355	261
230	VCOM	7172.5	-285	280	G90	6741	126	330	G190	6041	126	380	G290	5341	126
231	DUMMY	7232.5	-285	281	G92	6727	261	331	G192	6027	261	381	G292	5327	261
232	DUMMY	7292.5	-285	282	G94	6713	126	332	G194	6013	126	382	G294	5313	126
233	DUMMY	7399	261	283	G96	6699	261	333	G196	5999	261	383	G296	5299	261
234	DUMMY	7385	126	284	G98	6685	126	334	G198	5985	126	384	G298	5285	126
235	DUMMY	7371	261	285	G100	6671	261	335	G200	5971	261	385	G300	5271	261
236	G2	7357	126	286	G102	6657	126	336	G202	5957	126	386	G302	5257	126
237	G4	7343	261	287	G104	6643	261	337	G204	5943	261	387	G304	5243	261
238	G6	7329	126	288	G106	6629	126	338	G206	5929	126	388	G306	5229	126
239	G8	7315	261	289	G108	6615	261	339	G208	5915	261	389	G308	5215	261
240	G10	7301	126	290	G110	6601	126	340	G210	5901	126	390	G310	5201	126
241	G12	7287	261	291	G112	6587	261	341	G212	5887	261	391	G312	5187	261
242	G14	7273	126	292	G114	6573	126	342	G214	5873	126	392	G314	5173	126
243	G16	7259	261	293	G116	6559	261	343	G216	5859	261	393	G316	5159	261
244	G18	7245	126	294	G118	6545	126	344	G218	5845	126	394	G318	5145	126
245	G20	7231	261	295	G120	6531	261	345	G220	5831	261	395	G320	5131	261
246	G22	7217	126	296	G122	6517	126	346	G222	5817	126	396	S720	5075	126
247	G24	7203	261	297	G124	6503	261	347	G224	5803	261	397	S719	5061	261
248	G26	7189	126	298	G126	6489	126	348	G226	5789	126	398	S718	5047	126
249	G28	7175	261	299	G128	6475	261	349	G228	5775	261	399	S717	5033	261
250	G30	7161	126	300	G130	6461	126	350	G230	5761	126	400	S716	5019	126

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
401	S715	5005	261	451	S665	4305	261	501	S615	3605	261	551	S565	2905	261
402	S714	4991	126	452	S664	4291	126	502	S614	3591	126	552	S564	2891	126
403	S713	4977	261	453	S663	4277	261	503	S613	3577	261	553	S563	2877	261
404	S712	4963	126	454	S662	4263	126	504	S612	3563	126	554	S562	2863	126
405	S711	4949	261	455	S661	4249	261	505	S611	3549	261	555	S561	2849	261
406	S710	4935	126	456	S660	4235	126	506	S610	3535	126	556	S560	2835	126
407	S709	4921	261	457	S659	4221	261	507	S609	3521	261	557	S559	2821	261
408	S708	4907	126	458	S658	4207	126	508	S608	3507	126	558	S558	2807	126
409	S707	4893	261	459	S657	4193	261	509	S607	3493	261	559	S557	2793	261
410	S706	4879	126	460	S656	4179	126	510	S606	3479	126	560	S556	2779	126
411	S705	4865	261	461	S655	4165	261	511	S605	3465	261	561	S555	2765	261
412	S704	4851	126	462	S654	4151	126	512	S604	3451	126	562	S554	2751	126
413	S703	4837	261	463	S653	4137	261	513	S603	3437	261	563	S553	2737	261
414	S702	4823	126	464	S652	4123	126	514	S602	3423	126	564	S552	2723	126
415	S701	4809	261	465	S651	4109	261	515	S601	3409	261	565	S551	2709	261
416	S700	4795	126	466	S650	4095	126	516	S600	3395	126	566	S550	2695	126
417	S699	4781	261	467	S649	4081	261	517	S599	3381	261	567	S549	2681	261
418	S698	4767	126	468	S648	4067	126	518	S598	3367	126	568	S548	2667	126
419	S697	4753	261	469	S647	4053	261	519	S597	3353	261	569	S547	2653	261
420	S696	4739	126	470	S646	4039	126	520	S596	3339	126	570	S546	2639	126
421	S695	4725	261	471	S645	4025	261	521	S595	3325	261	571	S545	2625	261
422	S694	4711	126	472	S644	4011	126	522	S594	3311	126	572	S544	2611	126
423	S693	4697	261	473	S643	3997	261	523	S593	3297	261	573	S543	2597	261
424	S692	4683	126	474	S642	3983	126	524	S592	3283	126	574	S542	2583	126
425	S691	4669	261	475	S641	3969	261	525	S591	3269	261	575	S541	2569	261
426	S690	4655	126	476	S640	3955	126	526	S590	3255	126	576	S540	2555	126
427	S689	4641	261	477	S639	3941	261	527	S589	3241	261	577	S539	2541	261
428	S688	4627	126	478	S638	3927	126	528	S588	3227	126	578	S538	2527	126
429	S687	4613	261	479	S637	3913	261	529	S587	3213	261	579	S537	2513	261
430	S686	4599	126	480	S636	3899	126	530	S586	3199	126	580	S536	2499	126
431	S685	4585	261	481	S635	3885	261	531	S585	3185	261	581	S535	2485	261
432	S684	4571	126	482	S634	3871	126	532	S584	3171	126	582	S534	2471	126
433	S683	4557	261	483	S633	3857	261	533	S583	3157	261	583	S533	2457	261
434	S682	4543	126	484	S632	3843	126	534	S582	3143	126	584	S532	2443	126
435	S681	4529	261	485	S631	3829	261	535	S581	3129	261	585	S531	2429	261
436	S680	4515	126	486	S630	3815	126	536	S580	3115	126	586	S530	2415	126
437	S679	4501	261	487	S629	3801	261	537	S579	3101	261	587	S529	2401	261
438	S678	4487	126	488	S628	3787	126	538	S578	3087	126	588	S528	2387	126
439	S677	4473	261	489	S627	3773	261	539	S577	3073	261	589	S527	2373	261
440	S676	4459	126	490	S626	3759	126	540	S576	3059	126	590	S526	2359	126
441	S675	4445	261	491	S625	3745	261	541	S575	3045	261	591	S525	2345	261
442	S674	4431	126	492	S624	3731	126	542	S574	3031	126	592	S524	2331	126
443	S673	4417	261	493	S623	3717	261	543	S573	3017	261	593	S523	2317	261
444	S672	4403	126	494	S622	3703	126	544	S572	3003	126	594	S522	2303	126
445	S671	4389	261	495	S621	3689	261	545	S571	2989	261	595	S521	2289	261
446	S670	4375	126	496	S620	3675	126	546	S570	2975	126	596	S520	2275	126
447	S669	4361	261	497	S619	3661	261	547	S569	2961	261	597	S519	2261	261
448	S668	4347	126	498	S618	3647	126	548	S568	2947	126	598	S518	2247	126
449	S667	4333	261	499	S617	3633	261	549	S567	2933	261	599	S517	2233	261
450	S666	4319	126	500	S616	3619	126	550	S566	2919	126	600	S516	2219	126

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
601	S515	2205	261	651	S465	1505	261	701	S415	805	261	751	S365	105	261
602	S514	2191	126	652	S464	1491	126	702	S414	791	126	752	S364	91	126
603	S513	2177	261	653	S463	1477	261	703	S413	777	261	753	S363	77	261
604	S512	2163	126	654	S462	1463	126	704	S412	763	126	754	S362	63	126
605	S511	2149	261	655	S461	1449	261	705	S411	749	261	755	S361	49	261
606	S510	2135	126	656	S460	1435	126	706	S410	735	126	756	S360	-49	126
607	S509	2121	261	657	S459	1421	261	707	S409	721	261	757	S359	-63	261
608	S508	2107	126	658	S458	1407	126	708	S408	707	126	758	S358	-77	126
609	S507	2093	261	659	S457	1393	261	709	S407	693	261	759	S357	-91	261
610	S506	2079	126	660	S456	1379	126	710	S406	679	126	760	S356	-105	126
611	S505	2065	261	661	S455	1365	261	711	S405	665	261	761	S355	-119	261
612	S504	2051	126	662	S454	1351	126	712	S404	651	126	762	S354	-133	126
613	S503	2037	261	663	S453	1337	261	713	S403	637	261	763	S353	-147	261
614	S502	2023	126	664	S452	1323	126	714	S402	623	126	764	S352	-161	126
615	S501	2009	261	665	S451	1309	261	715	S401	609	261	765	S351	-175	261
616	S500	1995	126	666	S450	1295	126	716	S400	595	126	766	S350	-189	126
617	S499	1981	261	667	S449	1281	261	717	S399	581	261	767	S349	-203	261
618	S498	1967	126	668	S448	1267	126	718	S398	567	126	768	S348	-217	126
619	S497	1953	261	669	S447	1253	261	719	S397	553	261	769	S347	-231	261
620	S496	1939	126	670	S446	1239	126	720	S396	539	126	770	S346	-245	126
621	S495	1925	261	671	S445	1225	261	721	S395	525	261	771	S345	-259	261
622	S494	1911	126	672	S444	1211	126	722	S394	511	126	772	S344	-273	126
623	S493	1897	261	673	S443	1197	261	723	S393	497	261	773	S343	-287	261
624	S492	1883	126	674	S442	1183	126	724	S392	483	126	774	S342	-301	126
625	S491	1869	261	675	S441	1169	261	725	S391	469	261	775	S341	-315	261
626	S490	1855	126	676	S440	1155	126	726	S390	455	126	776	S340	-329	126
627	S489	1841	261	677	S439	1141	261	727	S389	441	261	777	S339	-343	261
628	S488	1827	126	678	S438	1127	126	728	S388	427	126	778	S338	-357	126
629	S487	1813	261	679	S437	1113	261	729	S387	413	261	779	S337	-371	261
630	S486	1799	126	680	S436	1099	126	730	S386	399	126	780	S336	-385	126
631	S485	1785	261	681	S435	1085	261	731	S385	385	261	781	S335	-399	261
632	S484	1771	126	682	S434	1071	126	732	S384	371	126	782	S334	-413	126
633	S483	1757	261	683	S433	1057	261	733	S383	357	261	783	S333	-427	261
634	S482	1743	126	684	S432	1043	126	734	S382	343	126	784	S332	-441	126
635	S481	1729	261	685	S431	1029	261	735	S381	329	261	785	S331	-455	261
636	S480	1715	126	686	S430	1015	126	736	S380	315	126	786	S330	-469	126
637	S479	1701	261	687	S429	1001	261	737	S379	301	261	787	S329	-483	261
638	S478	1687	126	688	S428	987	126	738	S378	287	126	788	S328	-497	126
639	S477	1673	261	689	S427	973	261	739	S377	273	261	789	S327	-511	261
640	S476	1659	126	690	S426	959	126	740	S376	259	126	790	S326	-525	126
641	S475	1645	261	691	S425	945	261	741	S375	245	261	791	S325	-539	261
642	S474	1631	126	692	S424	931	126	742	S374	231	126	792	S324	-553	126
643	S473	1617	261	693	S423	917	261	743	S373	217	261	793	S323	-567	261
644	S472	1603	126	694	S422	903	126	744	S372	203	126	794	S322	-581	126
645	S471	1589	261	695	S421	889	261	745	S371	189	261	795	S321	-595	261
646	S470	1575	126	696	S420	875	126	746	S370	175	126	796	S320	-609	126
647	S469	1561	261	697	S419	861	261	747	S369	161	261	797	S319	-623	261
648	S468	1547	126	698	S418	847	126	748	S368	147	126	798	S318	-637	126
649	S467	1533	261	699	S417	833	261	749	S367	133	261	799	S317	-651	261
650	S466	1519	126	700	S416	819	126	750	S366	119	126	800	S316	-665	126

No.	Pad name	X	Y
801	S315	-679	261
802	S314	-693	126
803	S313	-707	261
804	S312	-721	126
805	S311	-735	261
806	S310	-749	126
807	S309	-763	261
808	S308	-777	126
809	S307	-791	261
810	S306	-805	126
811	S305	-819	261
812	S304	-833	126
813	S303	-847	261
814	S302	-861	126
815	S301	-875	261
816	S300	-889	126
817	S299	-903	261
818	S298	-917	126
819	S297	-931	261
820	S296	-945	126
821	S295	-959	261
822	S294	-973	126
823	S293	-987	261
824	S292	-1001	126
825	S291	-1015	261
826	S290	-1029	126
827	S289	-1043	261
828	S288	-1057	126
829	S287	-1071	261
830	S286	-1085	126
831	S285	-1099	261
832	S284	-1113	126
833	S283	-1127	261
834	S282	-1141	126
835	S281	-1155	261
836	S280	-1169	126
837	S279	-1183	261
838	S278	-1197	126
839	S277	-1211	261
840	S276	-1225	126
841	S275	-1239	261
842	S274	-1253	126
843	S273	-1267	261
844	S272	-1281	126
845	S271	-1295	261
846	S270	-1309	126
847	S269	-1323	261
848	S268	-1337	126
849	S267	-1351	261
850	S266	-1365	126
851	S265	-1379	261
852	S264	-1393	126
853	S263	-1407	261
854	S262	-1421	126
855	S261	-1435	261
856	S260	-1449	126
857	S259	-1463	261
858	S258	-1477	126
859	S257	-1491	261
860	S256	-1505	126
861	S255	-1519	261
862	S254	-1533	126
863	S253	-1547	261
864	S252	-1561	126
865	S251	-1575	261
866	S250	-1589	126
867	S249	-1603	261
868	S248	-1617	126
869	S247	-1631	261
870	S246	-1645	126
871	S245	-1659	261
872	S244	-1673	126
873	S243	-1687	261
874	S242	-1701	126
875	S241	-1715	261
876	S240	-1729	126
877	S239	-1743	261
878	S238	-1757	126
879	S237	-1771	261
880	S236	-1785	126
881	S235	-1799	261
882	S234	-1813	126
883	S233	-1827	261
884	S232	-1841	126
885	S231	-1855	261
886	S230	-1869	126
887	S229	-1883	261
888	S228	-1897	126
889	S227	-1911	261
890	S226	-1925	126
891	S225	-1939	261
892	S224	-1953	126
893	S223	-1967	261
894	S222	-1981	126
895	S221	-1995	261
896	S220	-2009	126
897	S219	-2023	261
898	S218	-2037	126
899	S217	-2051	261
900	S216	-2065	126
901	S215	-2079	261
902	S214	-2093	126
903	S213	-2107	261
904	S212	-2121	126
905	S211	-2135	261
906	S210	-2149	126
907	S209	-2163	261
908	S208	-2177	126
909	S207	-2191	261
910	S206	-2205	126
911	S205	-2219	261
912	S204	-2233	126
913	S203	-2247	261
914	S202	-2261	126
915	S201	-2275	261
916	S200	-2289	126
917	S199	-2303	261
918	S198	-2317	126
919	S197	-2331	261
920	S196	-2345	126
921	S195	-2359	261
922	S194	-2373	126
923	S193	-2387	261
924	S192	-2401	126
925	S191	-2415	261
926	S190	-2429	126
927	S189	-2443	261
928	S188	-2457	126
929	S187	-2471	261
930	S186	-2485	126
931	S185	-2499	261
932	S184	-2513	126
933	S183	-2527	261
934	S182	-2541	126
935	S181	-2555	261
936	S180	-2569	126
937	S179	-2583	261
938	S178	-2597	126
939	S177	-2611	261
940	S176	-2625	126
941	S175	-2639	261
942	S174	-2653	126
943	S173	-2667	261
944	S172	-2681	126
945	S171	-2695	261
946	S170	-2709	126
947	S169	-2723	261
948	S168	-2737	126
949	S167	-2751	261
950	S166	-2765	126
951	S165	-2779	261
952	S164	-2793	126
953	S163	-2807	261
954	S162	-2821	126
955	S161	-2835	261
956	S160	-2849	126
957	S159	-2863	261
958	S158	-2877	126
959	S157	-2891	261
960	S156	-2905	126
961	S155	-2919	261
962	S154	-2933	126
963	S153	-2947	261
964	S152	-2961	126
965	S151	-2975	261
966	S150	-2989	126
967	S149	-3003	261
968	S148	-3017	126
969	S147	-3031	261
970	S146	-3045	126
971	S145	-3059	261
972	S144	-3073	126
973	S143	-3087	261
974	S142	-3101	126
975	S141	-3115	261
976	S140	-3129	126
977	S139	-3143	261
978	S138	-3157	126
979	S137	-3171	261
980	S136	-3185	126
981	S135	-3199	261
982	S134	-3213	126
983	S133	-3227	261
984	S132	-3241	126
985	S131	-3255	261
986	S130	-3269	126
987	S129	-3283	261
988	S128	-3297	126
989	S127	-3311	261
990	S126	-3325	126
991	S125	-3339	261
992	S124	-3353	126
993	S123	-3367	261
994	S122	-3381	126
995	S121	-3395	261
996	S120	-3409	126
997	S119	-3423	261
998	S118	-3437	126
999	S117	-3451	261
1000	S116	-3465	126

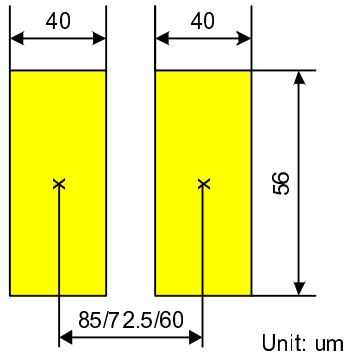
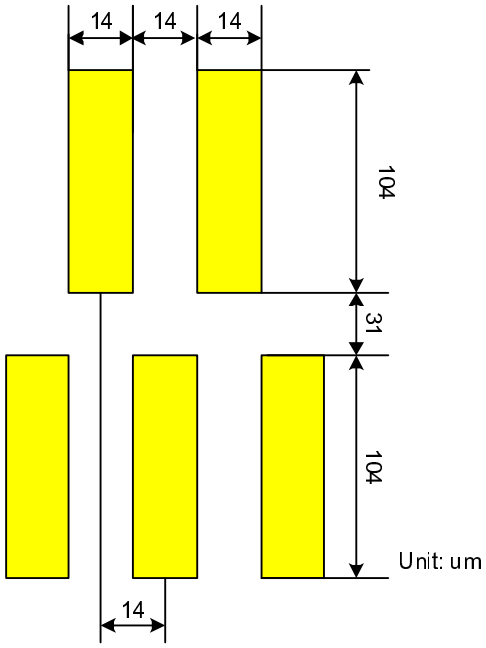
No.	Pad name	X	Y
1001	S115	-3479	261
1002	S114	-3493	126
1003	S113	-3507	261
1004	S112	-3521	126
1005	S111	-3535	261
1006	S110	-3549	126
1007	S109	-3563	261
1008	S108	-3577	126
1009	S107	-3591	261
1010	S106	-3605	126
1011	S105	-3619	261
1012	S104	-3633	126
1013	S103	-3647	261
1014	S102	-3661	126
1015	S101	-3675	261
1016	S100	-3689	126
1017	S99	-3703	261
1018	S98	-3717	126
1019	S97	-3731	261
1020	S96	-3745	126
1021	S95	-3759	261
1022	S94	-3773	126
1023	S93	-3787	261
1024	S92	-3801	126
1025	S91	-3815	261
1026	S90	-3829	126
1027	S89	-3843	261
1028	S88	-3857	126
1029	S87	-3871	261
1030	S86	-3885	126
1031	S85	-3899	261
1032	S84	-3913	126
1033	S83	-3927	261
1034	S82	-3941	126
1035	S81	-3955	261
1036	S80	-3969	126
1037	S79	-3983	261
1038	S78	-3997	126
1039	S77	-4011	261
1040	S76	-4025	126
1041	S75	-4039	261
1042	S74	-4053	126
1043	S73	-4067	261
1044	S72	-4081	126
1045	S71	-4095	261
1046	S70	-4109	126
1047	S69	-4123	261
1048	S68	-4137	126
1049	S67	-4151	261
1050	S66	-4165	126
1051	S65	-4179	261
1052	S64	-4193	126
1053	S63	-4207	261
1054	S62	-4221	126
1055	S61	-4235	261
1056	S60	-4249	126
1057	S59	-4263	261
1058	S58	-4277	126
1059	S57	-4291	261
1060	S56	-4305	126
1061	S55	-4319	261
1062	S54	-4333	126
1063	S53	-4347	261
1064	S52	-4361	126
1065	S51	-4375	261
1066	S50	-4389	126
1067	S49	-4403	261
1068	S48	-4417	126
1069	S47	-4431	261
1070	S46	-4445	126
1071	S45	-4459	261
1072	S44	-4473	126
1073	S43	-4487	261
1074	S42	-4501	126
1075	S41	-4515	261
1076	S40	-4529	126
1077	S39	-4543	261
1078	S38	-4557	126
1079	S37	-4571	261
1080	S36	-4585	126
1081	S35	-4599	261
1082	S34	-4613	126
1083	S33	-4627	261
1084	S32	-4641	126
1085	S31	-4655	261
1086	S30	-4669	126
1087	S29	-4683	261
1088	S28	-4697	126
1089	S27	-4711	261
1090	S26	-4725	126
1091	S25	-4739	261
1092	S24	-4753	126
1093	S23	-4767	261
1094	S22	-4781	126
1095	S21	-4795	261
1096	S20	-4809	126
1097	S19	-4823	261
1098	S18	-4837	126
1099	S17	-4851	261
1100	S16	-4865	126
1101	S15	-4879	261
1102	S14	-4893	126
1103	S13	-4907	261
1104	S12	-4921	126
1105	S11	-4935	261
1106	S10	-4949	126
1107	S9	-4963	261
1108	S8	-4977	126
1109	S7	-4991	261
1110	S6	-5005	126
1111	S5	-5019	261
1112	S4	-5033	126
1113	S3	-5047	261
1114	S2	-5061	126
1115	S1	-5075	261
1116	G319	-5131	126
1117	G317	-5145	261
1118	G315	-5159	126
1119	G313	-5173	261
1120	G311	-5187	126
1121	G309	-5201	261
1122	G307	-5215	126
1123	G305	-5229	261
1124	G303	-5243	126
1125	G301	-5257	261
1126	G299	-5271	126
1127	G297	-5285	261
1128	G295	-5299	126
1129	G293	-5313	261
1130	G291	-5327	126
1131	G289	-5341	261
1132	G287	-5355	126
1133	G285	-5369	261
1134	G283	-5383	126
1135	G281	-5397	261
1136	G279	-5411	126
1137	G277	-5425	261
1138	G275	-5439	126
1139	G273	-5453	261
1140	G271	-5467	126
1141	G269	-5481	261
1142	G267	-5495	126
1143	G265	-5509	261
1144	G263	-5523	126
1145	G261	-5537	261
1146	G259	-5551	126
1147	G257	-5565	261
1148	G255	-5579	126
1149	G253	-5593	261
1150	G251	-5607	126
1151	G249	-5621	261
1152	G247	-5635	126
1153	G245	-5649	261
1154	G243	-5663	126
1155	G241	-5677	261
1156	G239	-5691	126
1157	G237	-5705	261
1158	G235	-5719	126
1159	G233	-5733	261
1160	G231	-5747	126
1161	G229	-5761	261
1162	G227	-5775	126
1163	G225	-5789	261
1164	G223	-5803	126
1165	G221	-5817	261
1166	G219	-5831	126
1167	G217	-5845	261
1168	G215	-5859	126
1169	G213	-5873	261
1170	G211	-5887	126
1171	G209	-5901	261
1172	G207	-5915	126
1173	G205	-5929	261
1174	G203	-5943	126
1175	G201	-5957	261
1176	G199	-5971	126
1177	G197	-5985	261
1178	G195	-5999	126
1179	G193	-6013	261
1180	G191	-6027	126
1181	G189	-6041	261
1182	G187	-6055	126
1183	G185	-6069	261
1184	G183	-6083	126
1185	G181	-6097	261
1186	G179	-6111	126
1187	G177	-6125	261
1188	G175	-6139	126
1189	G173	-6153	261
1190	G171	-6167	126
1191	G169	-6181	261
1192	G167	-6195	126
1193	G165	-6209	261
1194	G163	-6223	126
1195	G161	-6237	261
1196	G159	-6251	126
1197	G157	-6265	261
1198	G155	-6279	126
1199	G153	-6293	261
1200	G151	-6307	126

No.	Pad name	X	Y
1201	G149	-6321	261
1202	G147	-6335	126
1203	G145	-6349	261
1204	G143	-6363	126
1205	G141	-6377	261
1206	G139	-6391	126
1207	G137	-6405	261
1208	G135	-6419	126
1209	G133	-6433	261
1210	G131	-6447	126
1211	G129	-6461	261
1212	G127	-6475	126
1213	G125	-6489	261
1214	G123	-6503	126
1215	G121	-6517	261
1216	G119	-6531	126
1217	G117	-6545	261
1218	G115	-6559	126
1219	G113	-6573	261
1220	G111	-6587	126
1221	G109	-6601	261
1222	G107	-6615	126
1223	G105	-6629	261
1224	G103	-6643	126
1225	G101	-6657	261
1226	G99	-6671	126
1227	G97	-6685	261
1228	G95	-6699	126
1229	G93	-6713	261
1230	G91	-6727	126
1231	G89	-6741	261
1232	G87	-6755	126
1233	G85	-6769	261
1234	G83	-6783	126
1235	G81	-6797	261
1236	G79	-6811	126
1237	G77	-6825	261
1238	G75	-6839	126
1239	G73	-6853	261
1240	G71	-6867	126
1241	G69	-6881	261
1242	G67	-6895	126
1243	G65	-6909	261
1244	G63	-6923	126
1245	G61	-6937	261
1246	G59	-6951	126
1247	G57	-6965	261
1248	G55	-6979	126
1249	G53	-6993	261
1250	G51	-7007	126

No.	Pad name	X	Y
1251	G49	-7021	261
1252	G47	-7035	126
1253	G45	-7049	261
1254	G43	-7063	126
1255	G41	-7077	261
1256	G39	-7091	126
1257	G37	-7105	261
1258	G35	-7119	126
1259	G33	-7133	261
1260	G31	-7147	126
1261	G29	-7161	261
1262	G27	-7175	126
1263	G25	-7189	261
1264	G23	-7203	126
1265	G21	-7217	261
1266	G19	-7231	126
1267	G17	-7245	261
1268	G15	-7259	126
1269	G13	-7273	261
1270	G11	-7287	126
1271	G9	-7301	261
1272	G7	-7315	126
1273	G5	-7329	261
1274	G3	-7343	126
1275	G1	-7357	261
1276	DUMMY	-7371	126
1277	DUMMY	-7385	261
1278	DUMMY	-7399	126

Alignment mark	X	Y
Left COG Align	-7480	260
Right COG Align	7480	260

BUMP Size

Input Pad (1 ~ 232)	
Output Pad (233 ~ 1278)	

6. Block Function Description

MCU System Interface

ILI9340 provides four kinds of MCU system interface with 8080-Ⅰ/8080-Ⅱ series parallel interface and 3-/4-line serial interface. The selection of the given interfaces are done by external IM [3:0] pins and shown as below:

IM3	IM2	IM1	IM0	MCU-Interface Mode	Pins in use	
					Register/Content	GRAM
0	0	0	0	8080 MCU 8-bit bus interface Ⅰ	D[7:0]	D[7:0],WRX,RDX,CSX,D/CX
0	0	0	1	8080 MCU 16-bit bus interface Ⅰ	D[7:0]	D[15:0] ,WRX,RDX,CSX,D/CX
0	0	1	0	8080 MCU 9-bit bus interface Ⅰ	D[7:0]	D[8:0] ,WRX,RDX,CSX,D/CX
0	0	1	1	8080 MCU 18-bit bus interface Ⅰ	D[7:0]	D[17:0] ,WRX,RDX,CSX,D/CX
0	1	0	1	3-wire 9-bit data serial interface Ⅰ	SCL,SDA,CSX	
0	1	1	0	4-wire 8-bit data serial interface Ⅰ	SCL,SDA,D/CX,CSX	
1	0	0	0	8080 MCU 16-bit bus interface Ⅱ	D[8:1]	D[17:10], D[8:1] , WRX,RDX,CSX,D/CX
1	0	0	1	8080 MCU 8-bit bus interface Ⅱ	D[17:10]	D[17:10], WRX,RDX,CSX,D/CX
1	0	1	0	8080 MCU 18-bit bus interface Ⅱ	D[8:1]	D[17:0] , WRX,RDX,CSX,D/CX D
1	0	1	1	8080 MCU 9-bit bus interface Ⅱ	D[17:10]	[17:9] , WRX,RDX,CSX,D/CX
1	1	0	1	3-wire 9-bit data serial interface Ⅱ	SCL,SDI,SDO, CSX	
1	1	1	0	4-wire 8-bit data serial interface Ⅱ	SCL,SDI,D/CX,SDO, CSX	

In 8080-Ⅰ/8080-Ⅱ series parallel interface, the registers are accessed by the D[17:0] data pins.

8080-Ⅰ Series				8080-Ⅱ Series				Operation
CSX	D/CX	RDX	WRX	CSX	D/CX	RDX	WRX	
"L"	"L"	"H"	⎍	"L"	"L"	"H"	⎍	Write command
"L"	"H"	⎍	"H"	"L"	"H"	⎍	"H"	Read parameter
"L"	"H"	"H"	⎍	"L"	"H"	"H"	⎍	Write parameter

Parallel RGB Interface

ILI9340 also supports the RGB interface for displaying a moving picture. When the RGB interface is selected, display operation is synchronized with externally signals, VSYNC, HSYNC, and DOTCLK and input display data is written in synchronization with these signals according to the polarity of enable signal (DE).

Graphic RAM (GRAM)

GRAM is a graphic RAM to store display data. GRAM size is 172,800 bytes with 18 bits per pixel for a maximum 240(RGB) x320 dot graphic display.

Grayscale Voltage Generating Circuit

Grayscale voltage generating circuit generates a liquid crystal drive voltage, which corresponds to grayscale level set in the gamma correction register. ILI9340 can display maximum 262,144 colors.

Power Supply Circuit

The LCD drive power supply circuit generates the voltage levels as GVDD, VGH, VGL and VCOM for driving TFT LCD panel.

Timing controller

The timing controller generates all the timing signals for display and GRAM access.

Oscillator

ILI9340 incorporates RC oscillator circuit and output a stable output frequency for operation.

Panel Driver Circuit

Liquid crystal display driver circuit consists of 720-output source driver (S1~S720), 320-output gate driver (G1~G320), and VCOM signal.

7. Function Description

7.1. MCU interfaces

ILI9340 provides the 8-/9-/16-/18-bit parallel system interface for 8080-Ⅰ/8080-Ⅱ series, and 3-/4-line serial system interface for serial data input. The input system interface is selected by external pins IM [3:0] and the bit formal per pixel color order is selected by DBI [2:0] bits of 3Ah register.

7.1.1. MCU interface selection

The selection of interface is done by setting external pins IM [3:0] as shown in the following table.

IM3	IM2	IM1	IM0	MCU-Interface Mode	Pins in use	
					Register/Content	GRAM
0	0	0	0	8080 MCU 8-bit bus interface Ⅰ	D[7:0]	D[7:0],WRX,RDX,CSX,D/CX
0	0	0	1	8080 MCU 16-bit bus interface Ⅰ	D[7:0]	D[15:0] ,WRX,RDX,CSX,D/CX
0	0	1	0	8080 MCU 9-bit bus interface Ⅰ	D[7:0]	D[8:0] ,WRX,RDX,CSX,D/CX
0	0	1	1	8080 MCU 18-bit bus interface Ⅰ	D[7:0]	D[17:0] ,WRX,RDX,CSX,D/CX
0	1	0	1	3-wire 9-bit data serial interface Ⅰ	SCL,SDA,CSX	
0	1	1	0	4-wire 8-bit data serial interface Ⅰ	SCL,SDA,D/CX,CSX	
1	0	0	0	8080 MCU 16-bit bus interface Ⅱ	D[8:1]	D[17:10], D[8:1] , WRX,RDX,CSX,D/CX
1	0	0	1	8080 MCU 8-bit bus interface Ⅱ	D[17:10]	D[17:10], WRX,RDX,CSX,D/CX
1	0	1	0	8080 MCU 18-bit bus interface Ⅱ	D[8:1]	D[17:0] , WRX,RDX,CSX,D/CX D
1	0	1	1	8080 MCU 9-bit bus interface Ⅱ	D[17:10]	[17:9] , WRX,RDX,CSX,D/CX
1	1	0	1	3-wire 9-bit data serial interface Ⅱ	SCL,SDI,SDO, CSX	
1	1	1	0	4-wire 8-bit data serial interface Ⅱ	SCL,SDI,D/CX,SDO, CSX	

7.1.2. 8080-Ⅰ Series Parallel Interface

ILI9340 can be accessed via 8-/9-/16-/18-bit MCU 8080-Ⅰ series parallel interface. The chip-select CSX (active low) is used to enable or disable ILI9340 chip. The RESX (active low) is an external reset signal. WRX is the parallel data write strobe, RDX is the parallel data read strobe and D[17:0] is parallel data bus.

ILI9340 latches the input data at the rising edge of WRX signal. The D/CX is the signal of data/command selection. When D/CX='1', D [17:0] bits are display RAM data or command's parameters. When D/CX='0', D [17:0] bits are commands.

The 8080-Ⅰ series bi-directional interface can be used for communication between the MCU controller and LCD driver chip. The 8080-Ⅰ Interface selection is done when IM3 pin is low state (VSS level). Interface bus width can be selected by IM [2:0] bits.

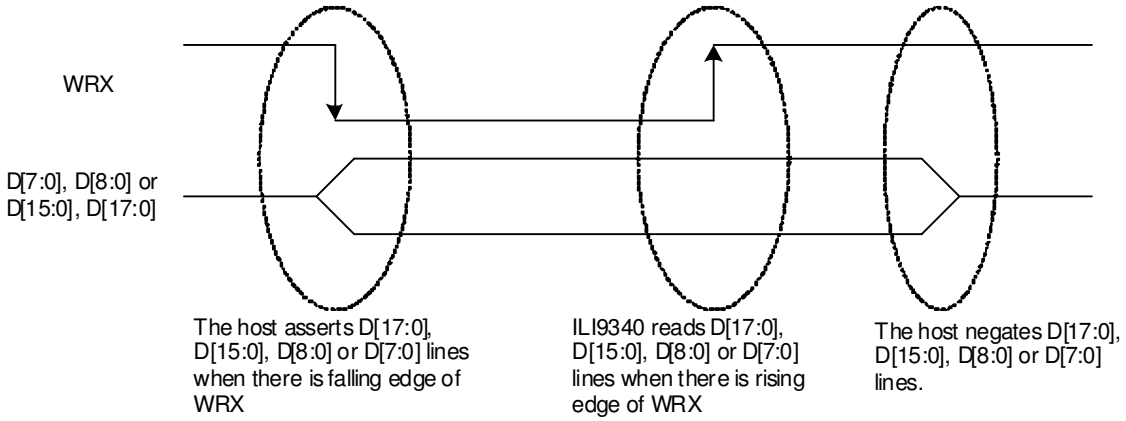
The selection of 8080-Ⅰ series parallel interface is shown as the table in the following.

IM3	IM2	IM1	IM0	MCU-Interface Mode	CSX	WRX	RDX	D/CX	Function
0	0	0	0	8080 MCU 8-bit bus interface Ⅰ	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.
0	0	0	1	8080 MCU 16-bit bus interface Ⅰ	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.
0	0	1	0	8080 MCU 9-bit bus interface Ⅰ	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.
0	0	1	1	8080 MCU 18-bit bus interface Ⅰ	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.

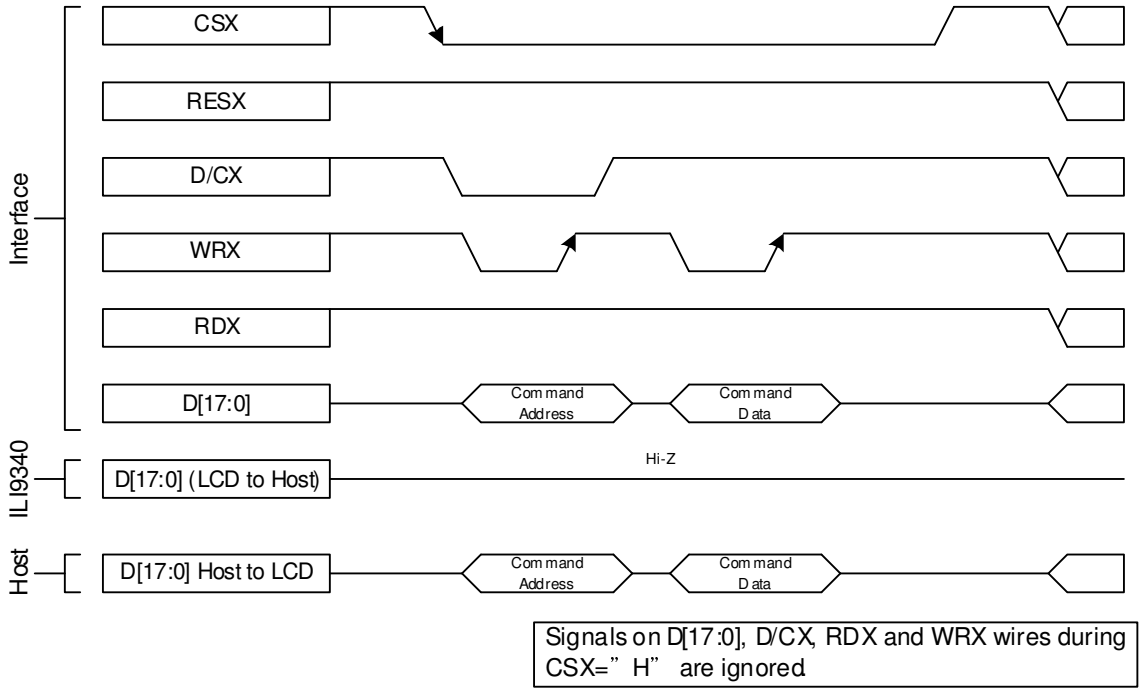
7.1.3. Write Cycle Sequence

The WRX signal is driven from high to low and then be pulled back to high during the write cycle. The host processor provides information during the write cycle when the display module captures the information from host processor on the rising edge of WRX. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command information. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command's parameter.

The following figure shows a write cycle for the 8080-Ⅰ MCU interface.



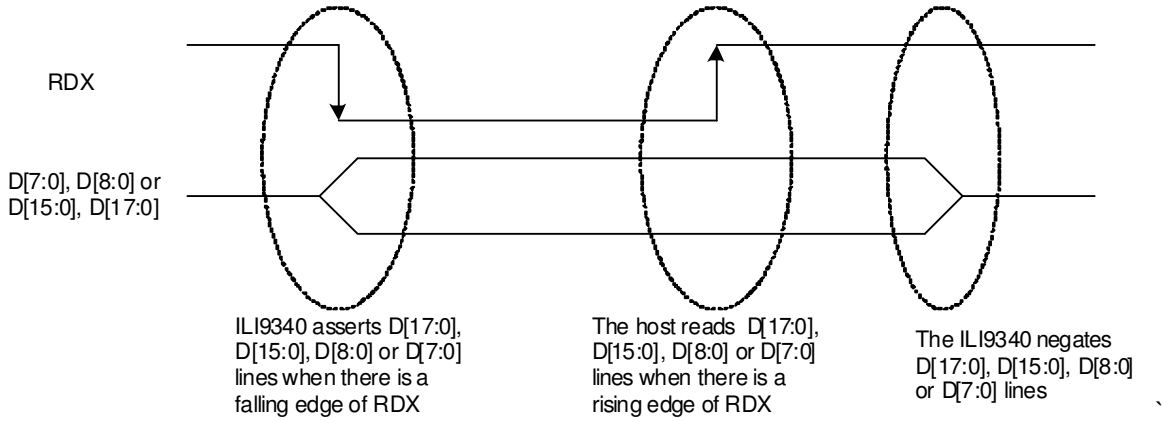
Note: WRX is an unsynchronized signal (It can be stopped)



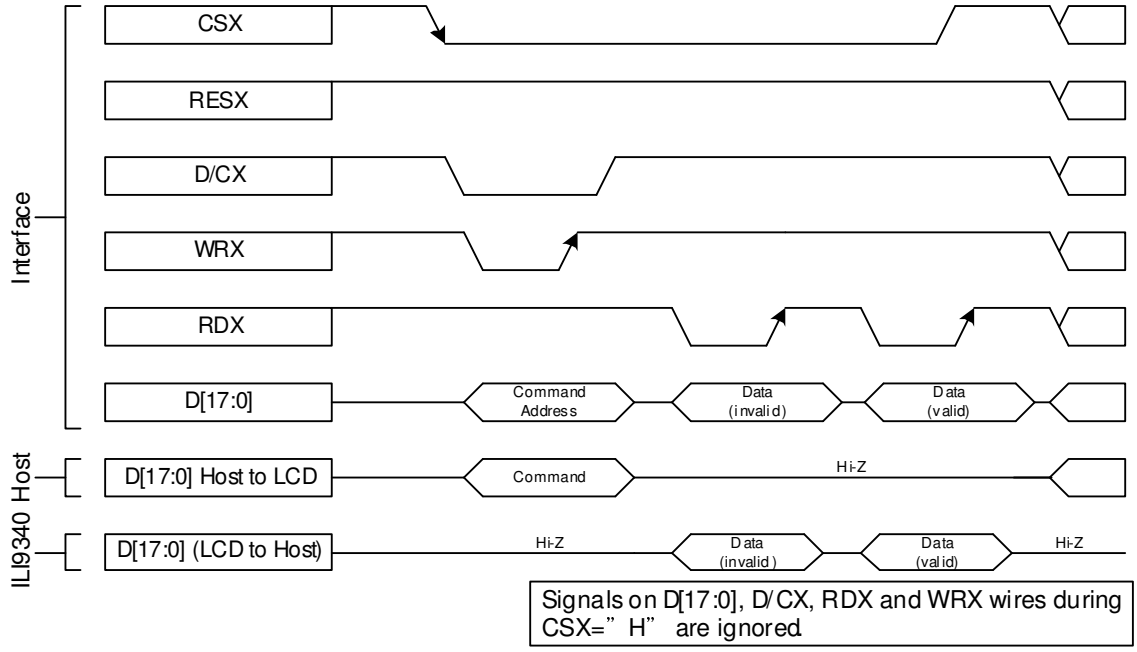
7.1.4. Read Cycle Sequence

The RDX signal is driven from high to low and then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle while the host processor reads the display module information on the rising edge of RDX signal. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command parameter.

The following figure shows the read cycle for the 8080-Ⅰ MCU interface.



Note: RDX is an unsynchronized signal (It can be stopped).



Note: Read data is only valid when the D/CX input is pulled high. If D/CX is driven low during read then the display information outputs will be High-Z.

7.1.5. 8080-Ⅱ Series Parallel Interface

ILI9340 can be accessed via 8-/9-/16-/18-bit MCU 8080-Ⅱ series parallel interface. The chip-select CSX (active low) is used to enable or disable ILI9340 chip. The RESX (active low) is an external reset signal. WRX is the parallel data write strobe, RDX is the parallel data read strobe and D[17:0] is parallel data bus.

ILI9340 latches the input data at the rising edge of WRX signal. The D/CX is the signal of data/command selection. When D/CX='1', D [17:0] bits are display RAM data or command's parameters. When D/CX='0', D [17:0] bits are commands.

The 8080-Ⅱ series bi-directional interface can be used for communication between the MCU controller and LCD driver chip. The 8080-Ⅱ Interface selection is done when IM3 pin is high state (VDDI level). Interface bus width can be selected by IM [2:0] bits.

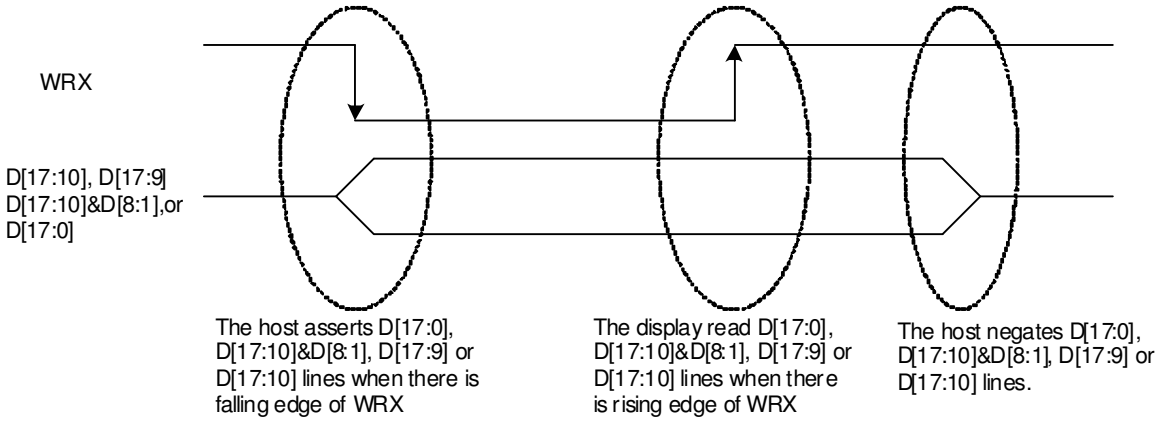
The selection of 8080-Ⅱ series parallel interface is shown as the table in the following.

IM3	IM2	IM1	IM0	MCU-Interface Mode	CSX	WRX	RDX	D/CX	Function
1	0	0	0	8080 MCU 16-bit bus interface Ⅱ	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.
1	0	0	1	8080 MCU 8-bit bus interface Ⅱ	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.
1	0	1	0	8080 MCU 18-bit bus interface Ⅱ	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.
1	0	1	1	8080 MCU 9-bit bus interface Ⅱ	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.

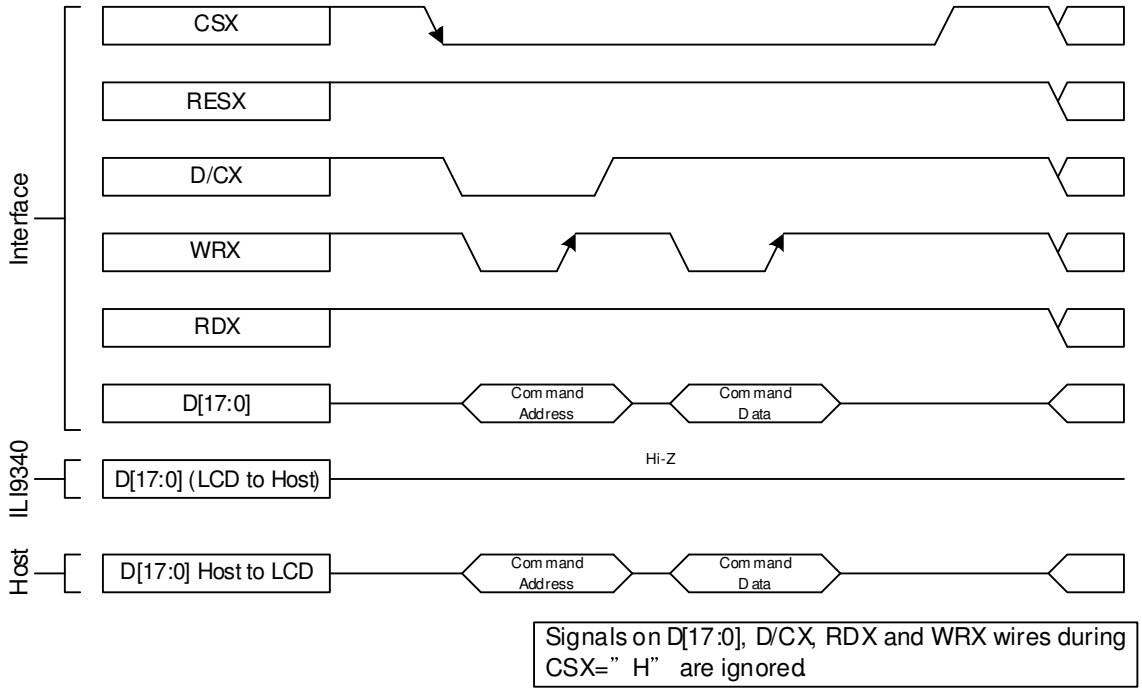
7.1.6. Write Cycle Sequence

The WRX signal is driven from high to low and then be pulled back to high during the write cycle. The host processor provides information during the write cycle when the display module captures the information from host processor on the rising edge of WRX. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command information. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command's parameter.

The following figure shows a write cycle for the 8080-Ⅱ MCU interface.



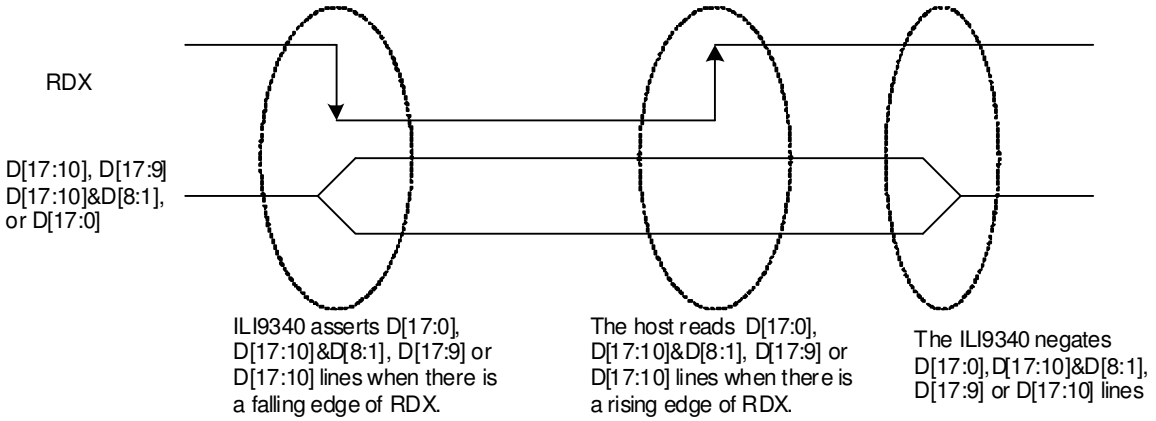
Note: WRX is an unsynchronized signal (It can be stopped)



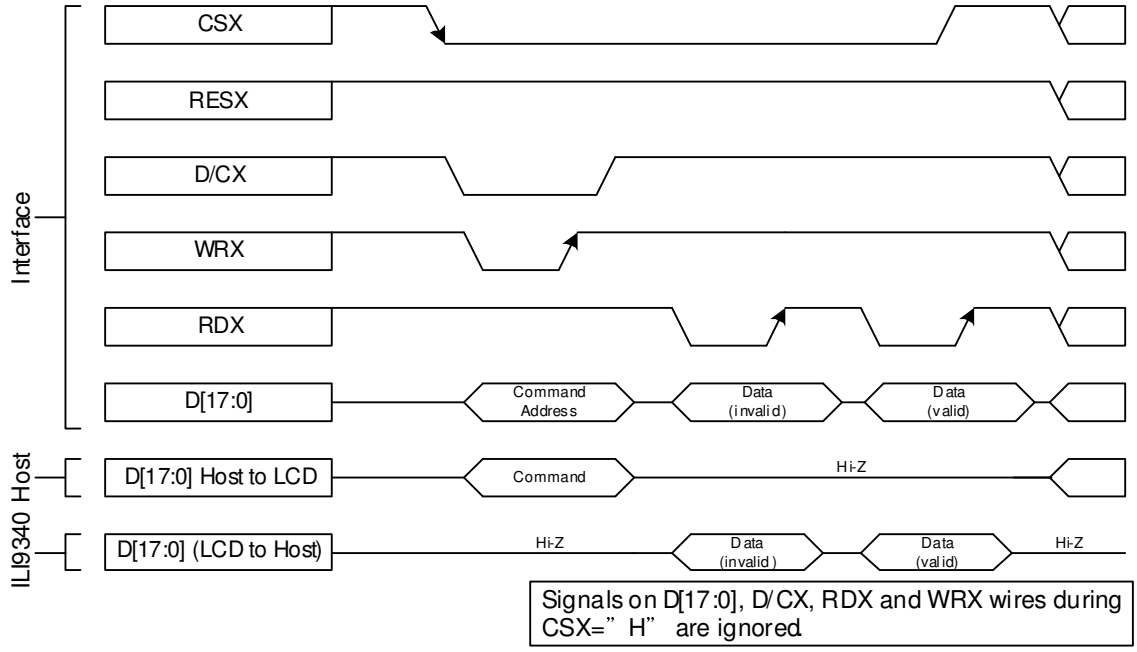
7.1.7. Read Cycle Sequence

The RDX signal is driven from high to low and then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle while the host processor reads the display module information on the rising edge of RDX signal. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command parameter.

The following figure shows the read cycle for the 8080-Ⅱ MCU interface.



Note: RDX is an unsynchronized signal (It can be stopped).



Note: Read data is only valid when the D/CX input is pulled high. If D/CX is driven low during read then the display information outputs will be High-Z.

7.1.8. Serial Interface

The selection of interface is done by IM [3:0] bits. Please refer to the Table in the following.

IM3	IM2	IM1	IM0	MCU-Interface Mode	CSX	D/CX	SCL	Function
0	1	0	1	3-line serial interface	"L"	-	⎍	Read/Write command, parameter or display data.
0	1	1	0	4-line serial interface	"L"	'H/L"	⎍	Read/Write command, parameter or display data.
1	1	0	1	3-line serial interface	"L"	-	⎍	Read/Write command, parameter or display data.
1	1	1	0	4-line serial interface	"L"	'H/L"	⎍	Read/Write command, parameter or display data.

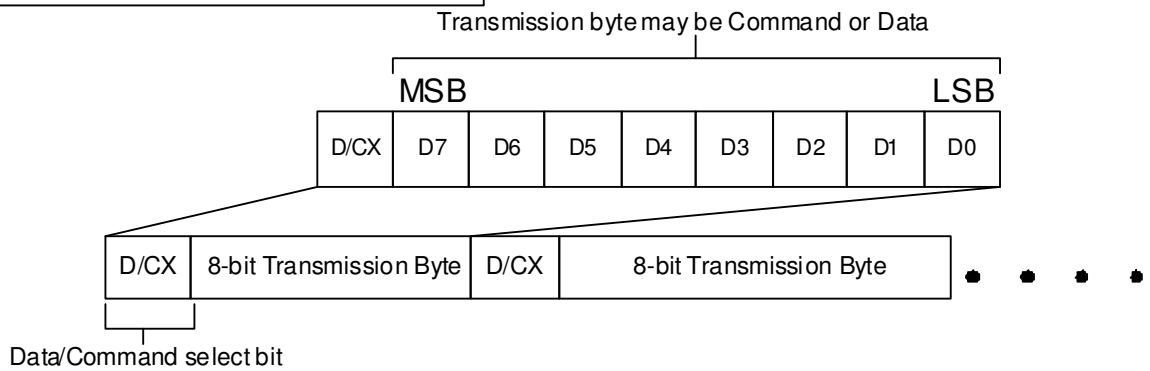
ILI9340 supplies 3-lines/ 9-bit and 4-line/8-bit bi-directional serial interfaces for communication between host and ILI9340. The 3-line serial mode consists of the chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA or SDI/SDO). The 4-line serial mode consists of the Data/Command selection input (D/CX), chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA or SDI/SDO) for data transmission. The data bus (D [17:0]), which are not used, must be connected to GND. Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

7.1.9. Write Cycle Sequence

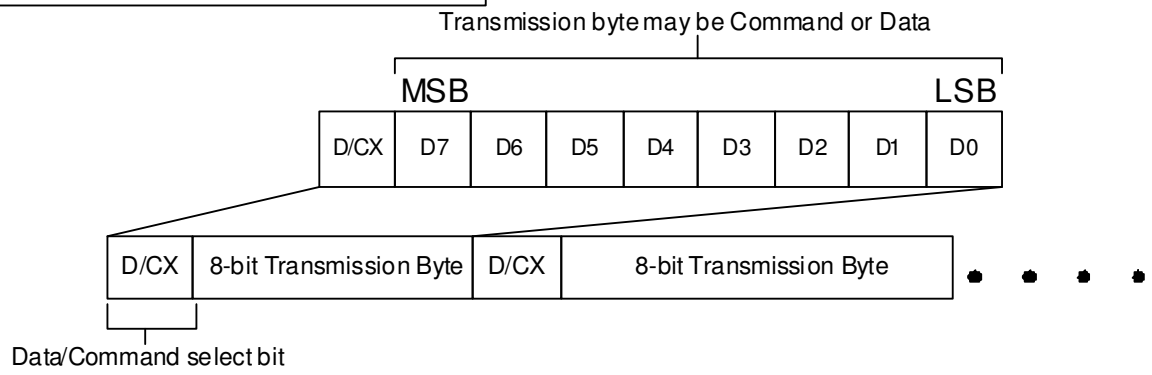
The write mode of the interface means that host writes commands or data to ILI9340. The 3-lines serial data packet contains a data/command select bit (D/CX) and a transmission byte. If the D/CX bit is "low", the transmission byte is interpreted as a command byte. If the D/CX bit is "high", the transmission byte is stored as the display data RAM (Memory write command), or command register as parameter.

Any instruction can be sent in any order to ILI9340 and the MSB is transmitted first. The serial interface is initialized when CSX is high status. In this state, SCL clock pulse and SDA data are no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission. See the detailed data format for 3-/4-line serial interface.

Data Format for 3-line Serial Interface

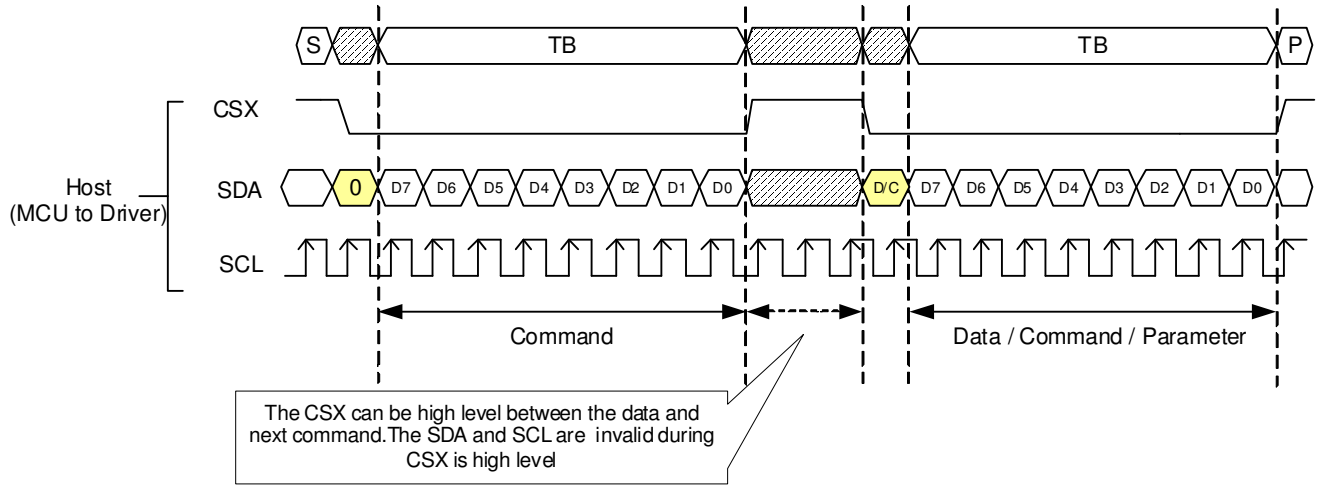


Data Format for 3-line Serial Interface

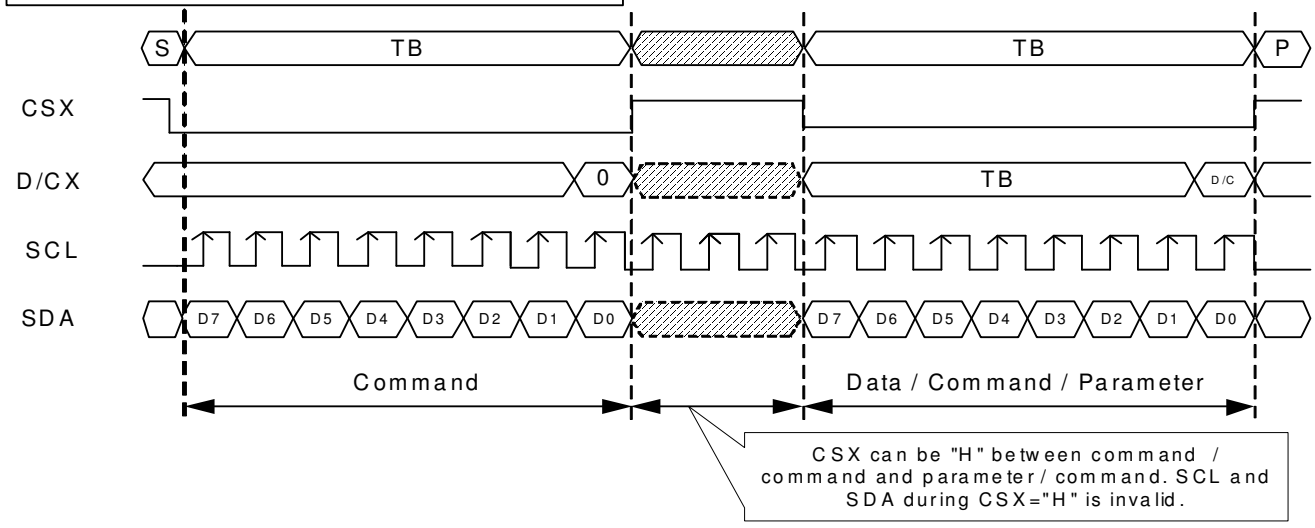


Host processor drives the CSX pin to low and starts by setting the D/CX bit on SDA. The bit is read by ILI9340 on the first rising edge of SCL signal. On the next falling edge of SCL, the MSB data bit (D7) is set on SDA by the host. On the next falling edge of SCL, the next bit (D6) is set on SDA. If the optional D/CX signal is used, a byte is eight read cycle width. The 3/4-line serial interface writes sequence described in the figure as below.

3-line Serial Interface Protocol



4-line Serial Interface Protocol

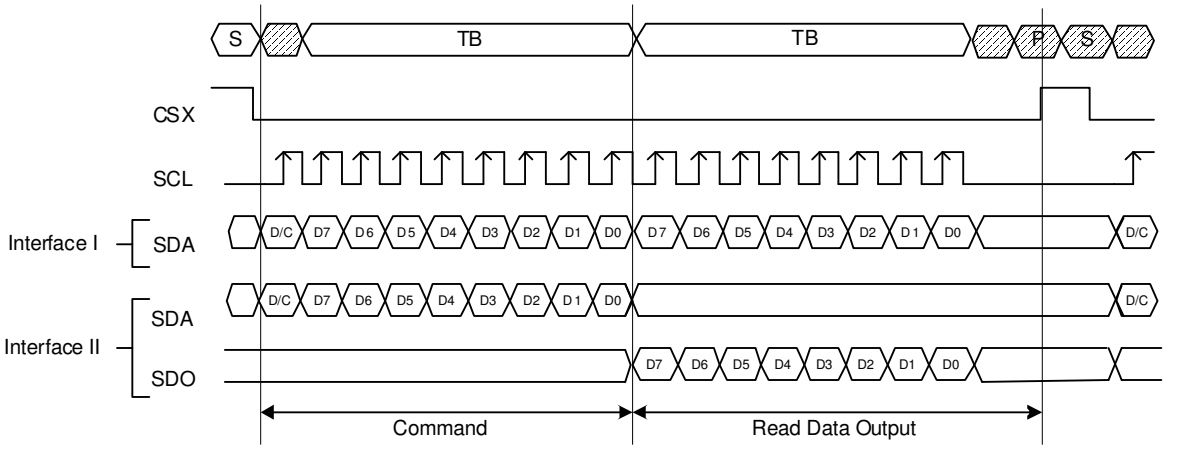


7.1.10. Read Cycle Sequence

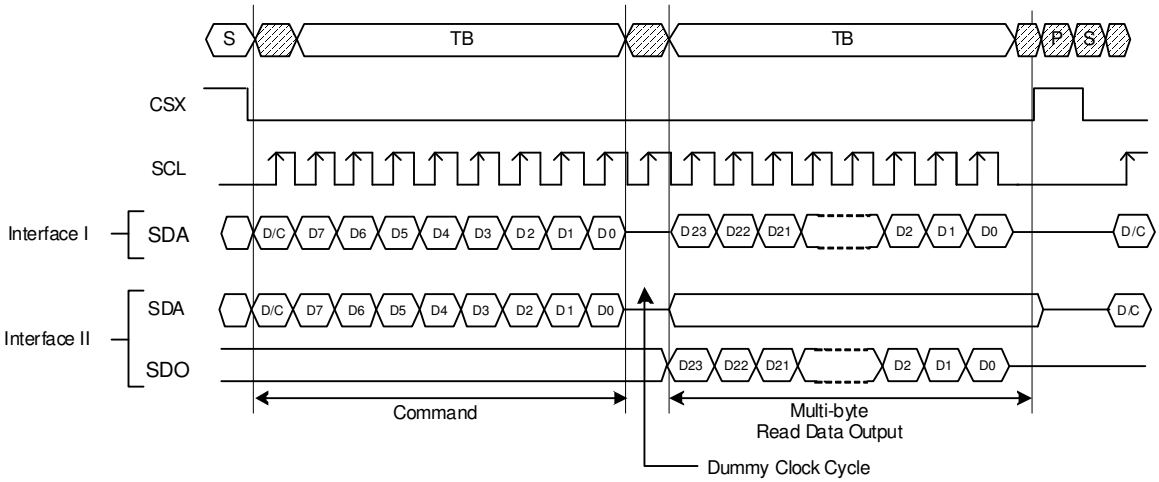
The read mode of interface means that the host reads register's parameter or display data from ILI9340. The host has to send a command (Read ID or register command) and then the following byte is transmitted in the opposite direction. ILI9340 latches the SDA (input data) at the rising edges of SCL (serial clock), and then shifts SDA (output data) at falling edges of SCL (serial clock). After the read status command has been sent, the SDA line must be set to tri-state and no later than at the falling edge of SCL of the last bit. The read mode has three types of transmitted command data (8-/24-/32-bit) according command code.

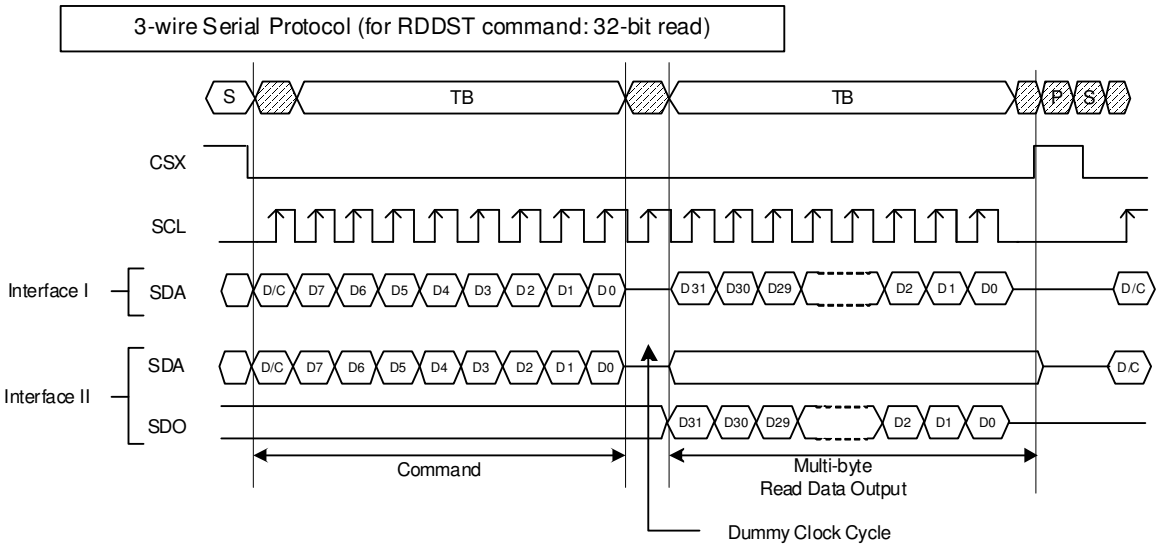
3-wire Serial Interface Protocol

3-wire Serial Protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read)



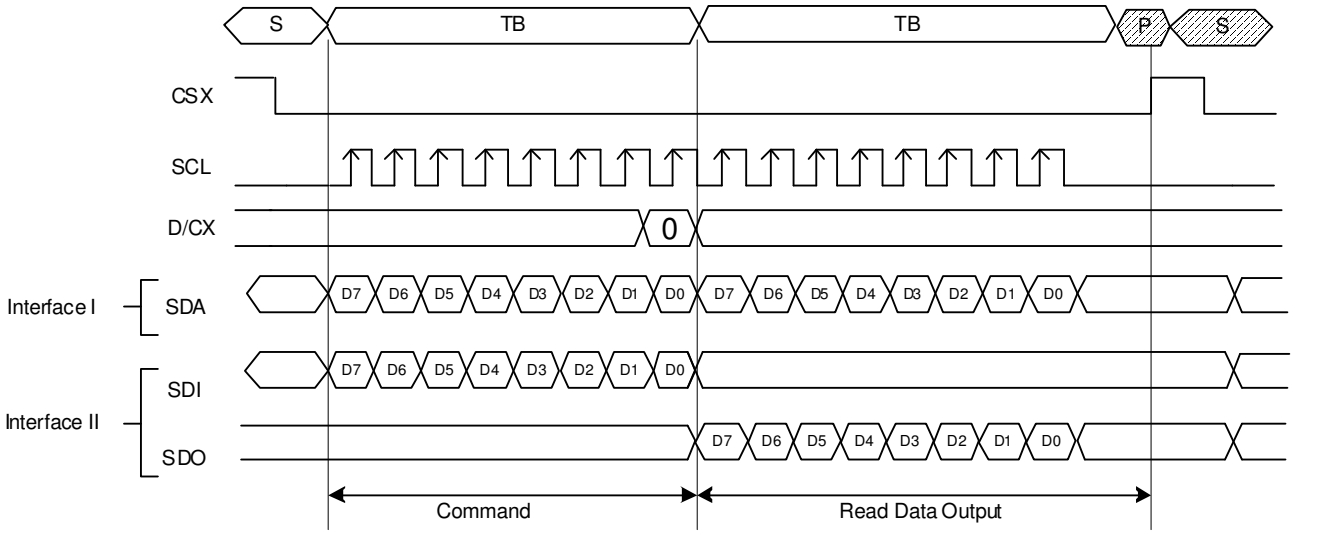
3-wire Serial Protocol (for RDDID command: 24-bit read)



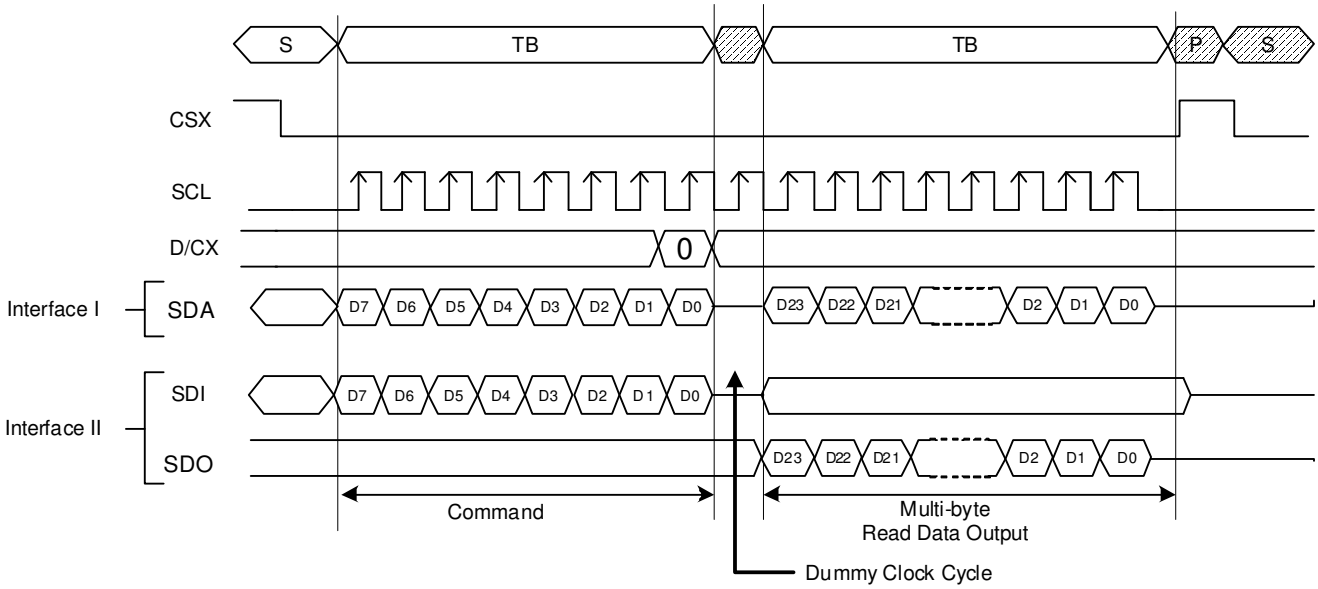


4-wire Serial Interface Protocol

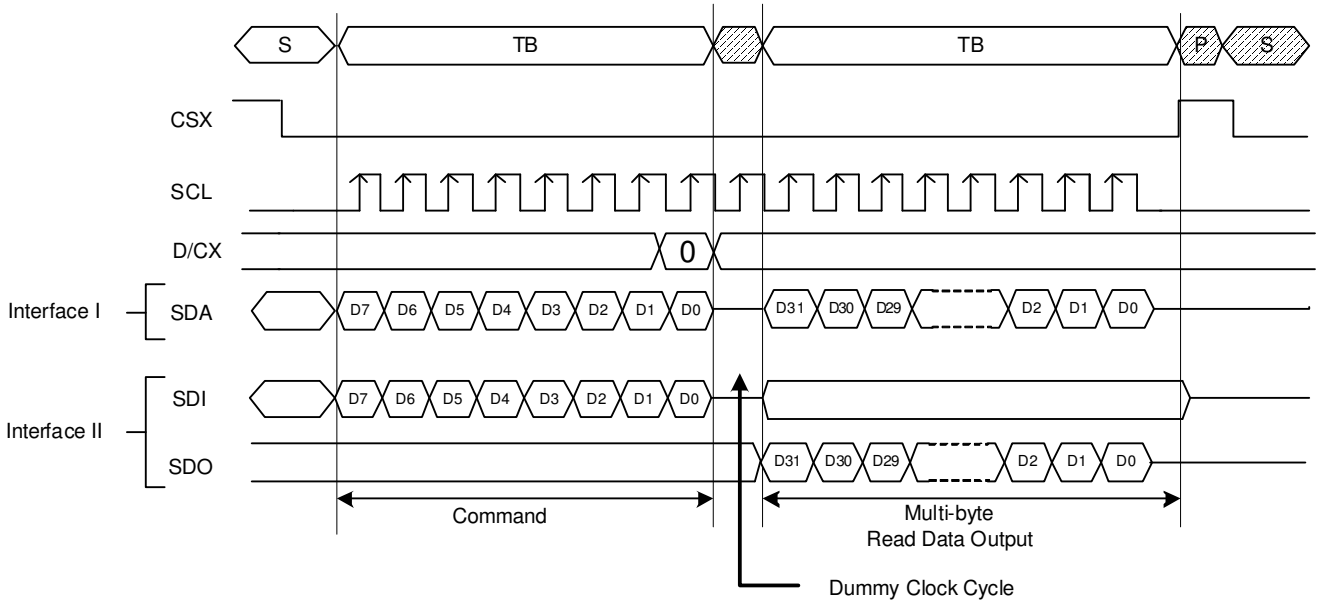
4-wire Serial Protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read)



4-wire Serial Protocol (for RDDID command: 24-bit read)

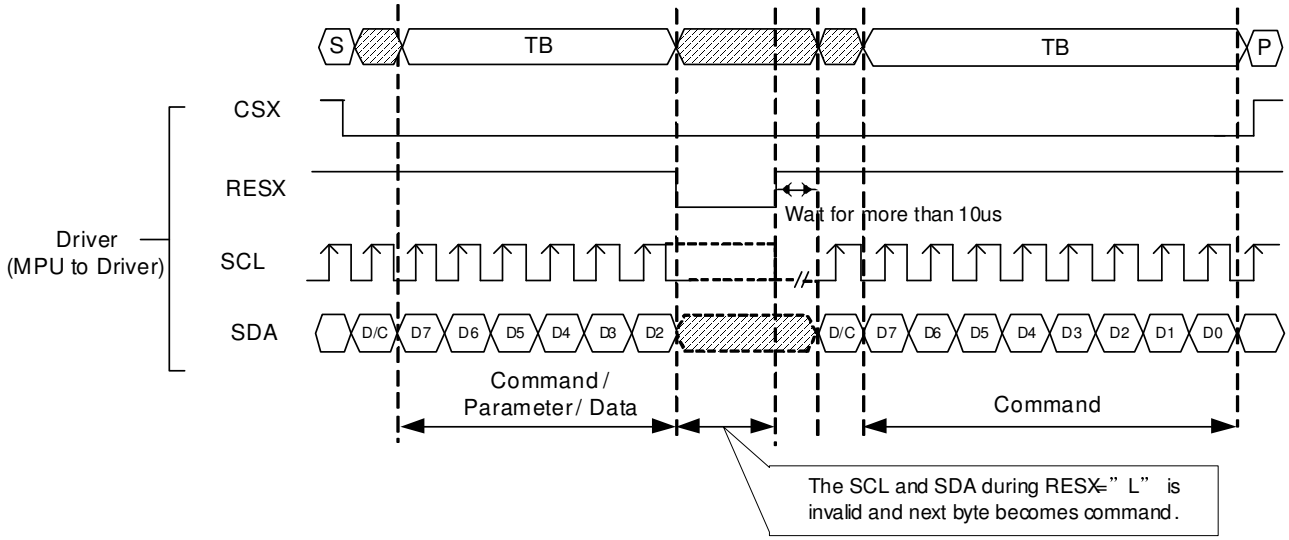


4-wire Serial Protocol (for RDDST command: 32-bit read)

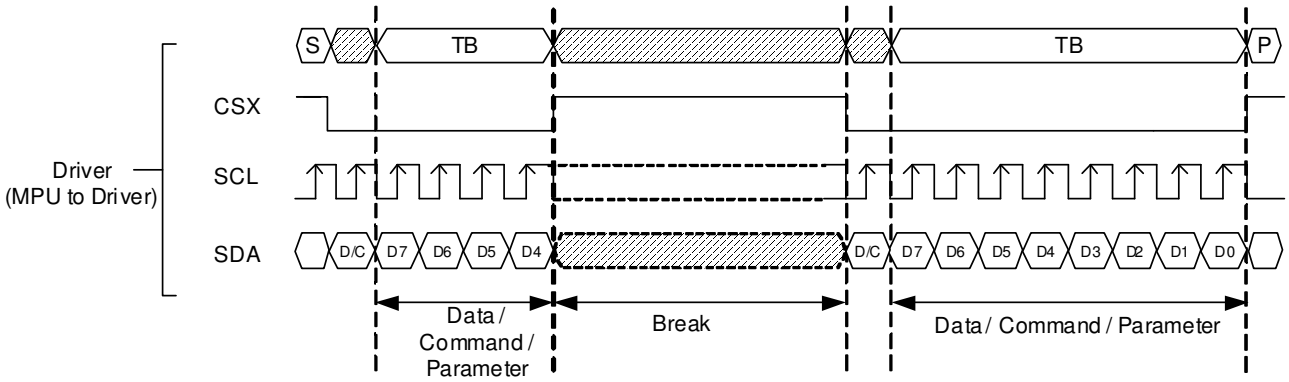


7.1.11. Data Transfer Break and Recovery

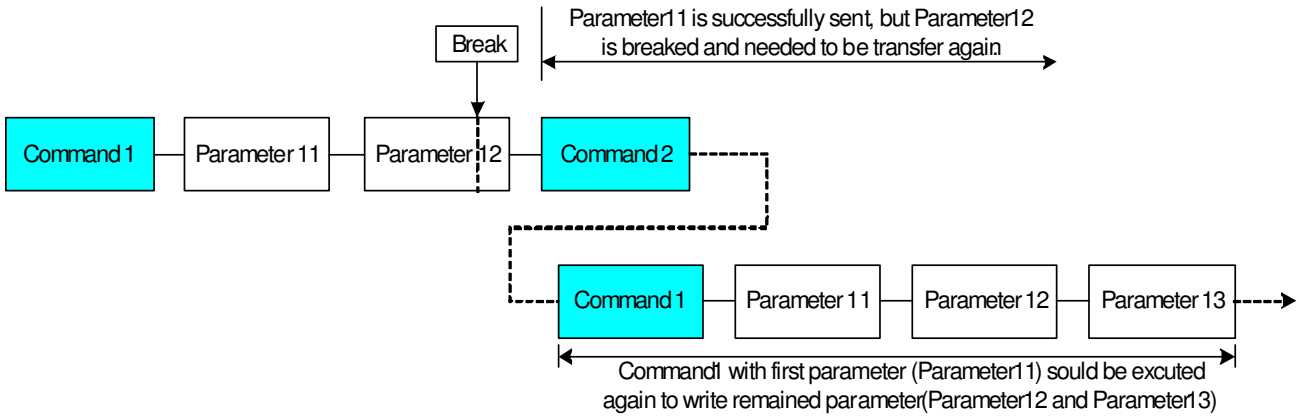
If there is a break in data transmission by RESX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select pin (CSX) is activated after RESX have been high state.



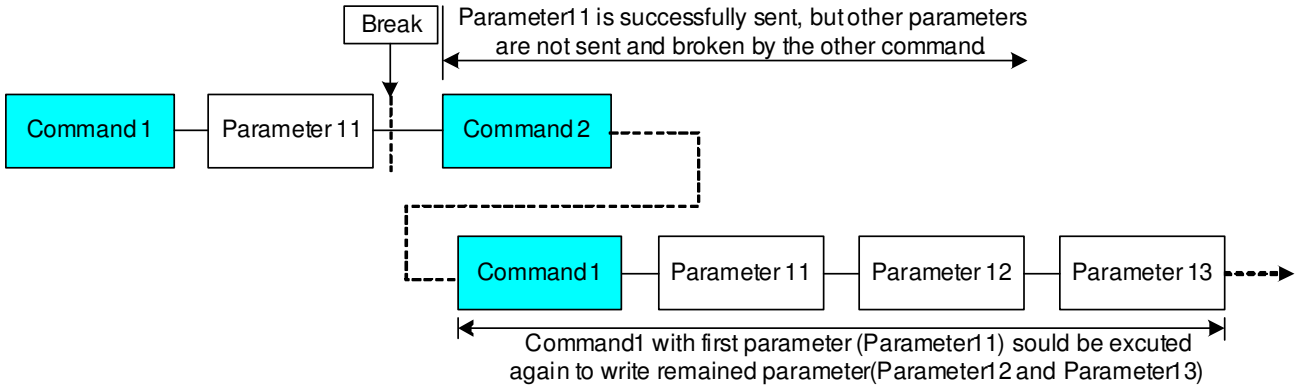
If there is a break in data transmission by CSX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select pin (CSX) is next activated.



If a two or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than continue to send the remained parameters that was interrupted, then the parameters which had been successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.



If a two or more parameter command is being sent and a break occurs by the other command before the last one is sent, then the parameters which had been successfully sent are stored and the other parameter of that command remains previous value.



7.1.12. Data Transfer Pause

It will be possible when transferring a command, frame memory data or multiple parameter data to invoke a pause in the data transmission. If the chip select pin (CSX) is released to high state after a whole byte of a frame memory data or multiple parameter data has been completed, then ILI9340 will wait and continue the frame memory data or parameter data transmission from the point where it was paused. If the chip select pin is released after a whole byte of a command has been completed, then the display module will receive either the command's parameters (if appropriate) or a new command when the chip select pin is next enabled as shown below.

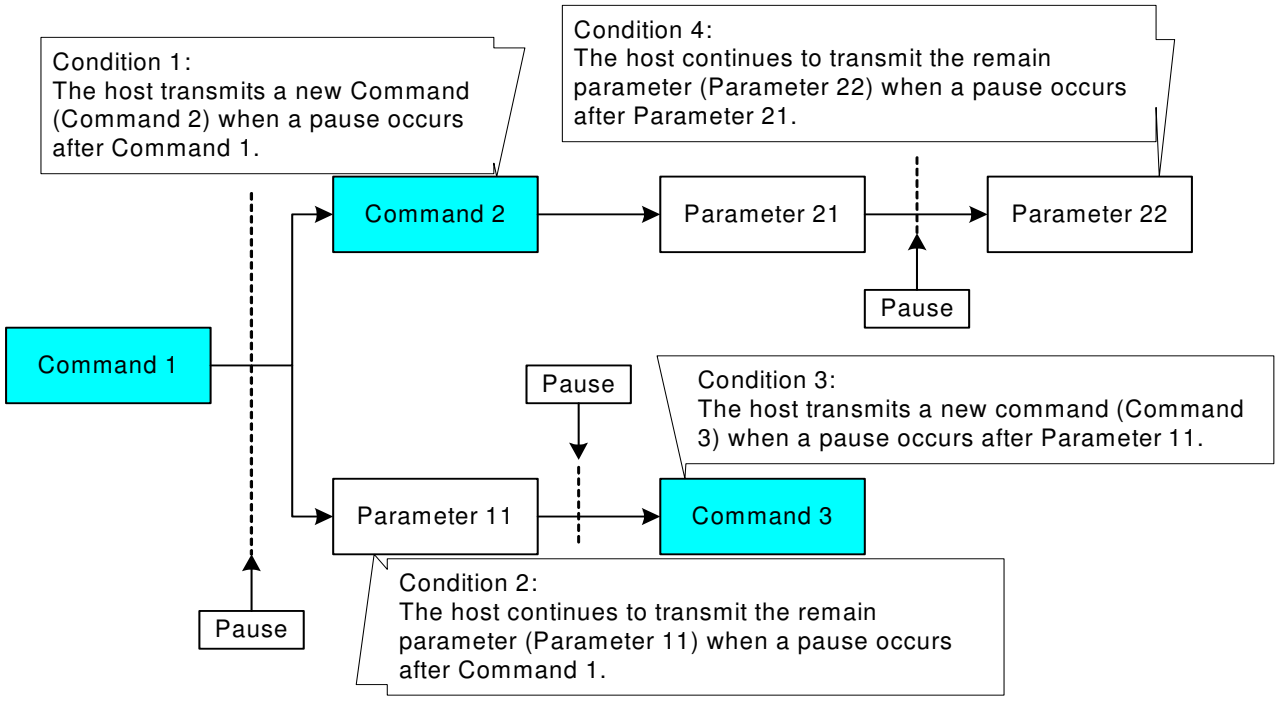
This applies to the following 4 conditions:

1) Command-Pause-Command

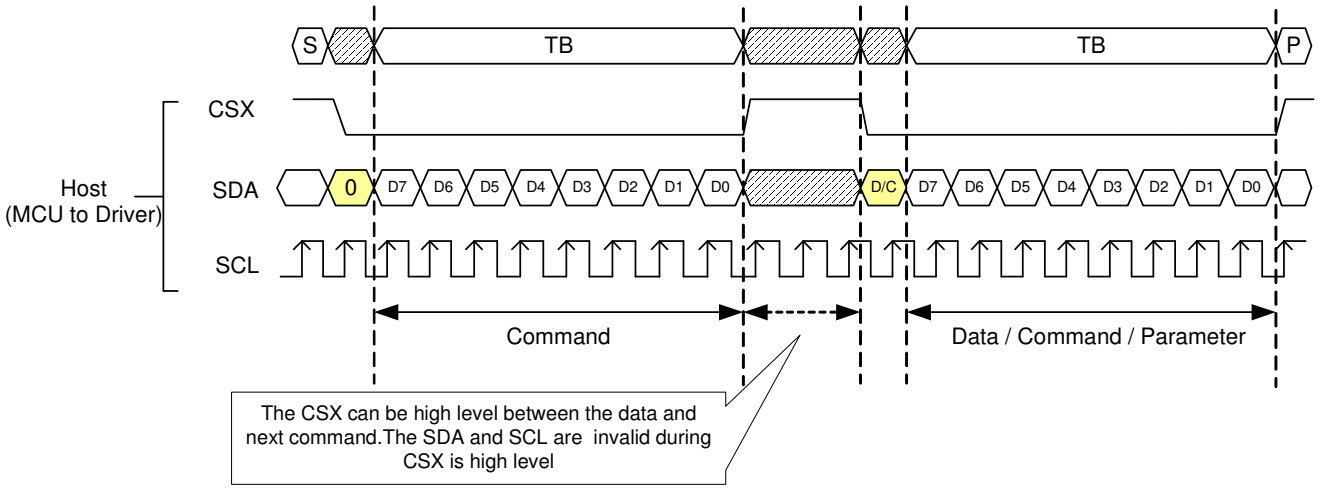
2) Command-Pause-Parameter

3) Parameter-Pause-Command

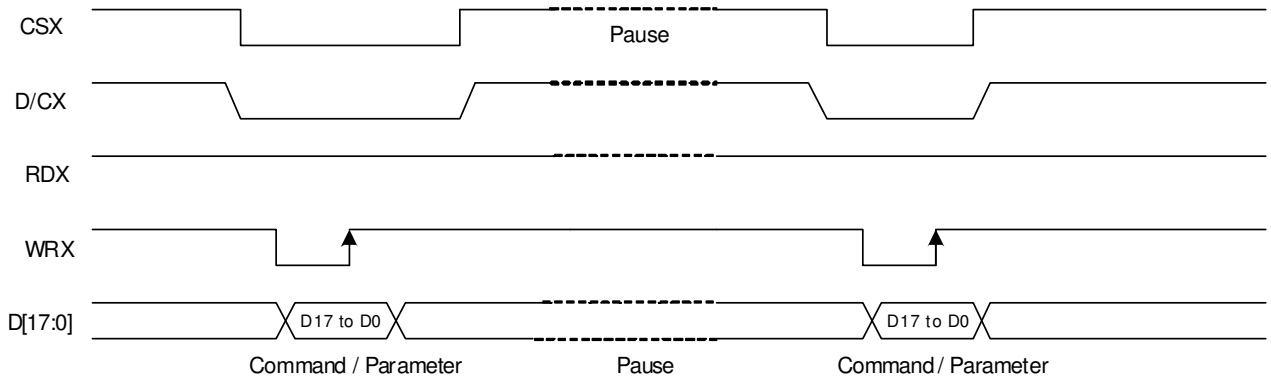
4) Parameter-Pause-Parameter



7.1.13. Serial Interface Pause (3_wire)



7.1.14. Parallel Interface Pause

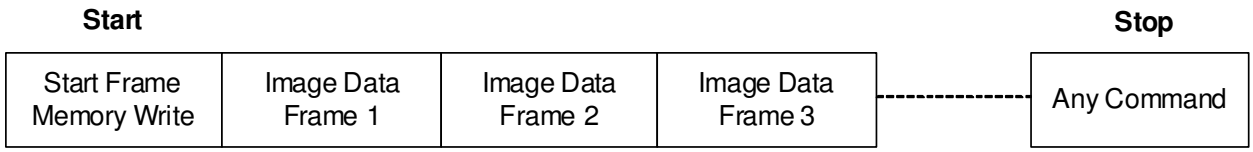


7.1.15. Data Transfer Mode

ILI9340 can provide two different kinds of color depth (16-bit/pixel and 18-bit/pixel) display data to the graphic RAM. The data format is described for each interface. Data can be downloaded to the frame memory by 2 methods.

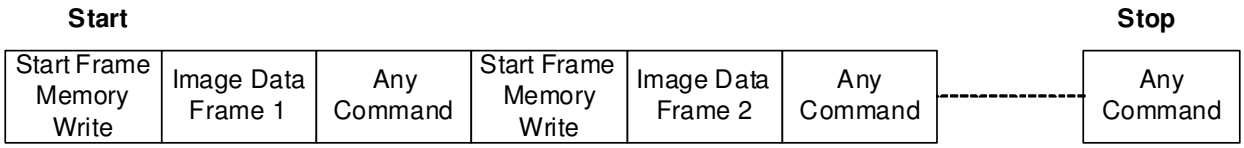
7.1.16. Data Transfer Method 1

The image data is sent to the frame memory in the successive frame writing, each time the frame memory is filled by image data, the frame memory pointer is reset to the start point and the next frame is written.



7.1.17. Data Transfer Method 2

Image data is sent and at the end of each frame memory download, a command is sent to stop frame memory writing. Then start memory write command is sent, and a new frame is downloaded.



Note 1: These methods are applied to all data transfer color modes on both serial and parallel interfaces.

Note 2: The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.

7.2. RGB Interface

7.2.1. RGB Interface Selection

ILI9340 has two kinds of RGB interface and these interfaces can be selected by RCM [1:0] bits. When RCM [1:0] bits are set to “10”, the DE mode is selected which utilizes VSYNC, HSYNC, DOTCLK, DE, D [17:0] pins; when RCM [1:0] bits are set to “11”, the SYNC mode is selected which utilizes which utilizes VSYNC, HSYNC, DOTCLK, D [17:0] pins. Using RGB interface must selection serial interface.

ILI9340 supports several pixel formats that can be selected by DPI [2:0] bits of “Pixel Format Set (3Ah)” and RIM bit of RF6h command. The selection of a given interfaces is done by setting RCM [1:0] and DPI [2:0] as show in the following table.

RCM[1:0]		RIM	DPI[2:0]			RGB Interface Mode	RGB Mode	Used Pins
1	0	0	1	1	0	18-bit RGB interface (262K colors)	**DE Mode** Valid data is determined by the DE signal	VSYNC, HSYNC, DE, DOTCLK,D[17:0]
1	0	0	1	0	1	16-bit RGB interface (65K colors)		VSYNC, HSYNC, DE, DOTCLK, D[17:13] & D[11:1]
1	0	1	1	1	0	6-bit RGB interface (262K colors)		VSYNC, HSYNC, DE, DOTCLK, D[5:0]
1	0	1	1	0	1	6-bit RGB interface (65K colors)		VSYNC, HSYNC, DE, DOTCLK, D[5:0]
1	1	0	1	1	0	18-bit RGB interface (262K colors)	**SYNC Mode** In SYNC mode, DE signal is ignored; blanking porch is determined by B5h command.	VSYNC, HSYNC, DOTCLK, D[17:0]
1	1	0	1	0	1	16-bit RGB interface (65K colors)		VSYNC, HSYNC, DOTCLK, D[17:13] & D[11:1]
1	1	1	1	1	0	6-bit RGB interface (262K colors)		VSYNC, HSYNC, DOTCLK, D[5:0]
1	1	1	1	0	1	6-bit RGB interface (65K colors)		VSYNC, HSYNC, DOTCLK, D[5:0]

18-bit data bus interface (D[17:0] is used) , DPI[2:0] = 110 , and RIM=0

	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
18bpp Frame Memory Write	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

16-bit data bus interface (D[17:13] & D[11:1] is used) , DPI[2:0] = 101 , and RIM=0

	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
16bpp Frame Memory Write	R[4]	R[3]	R[2]	R[1]	R[0]		G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	

The LSB data of red/blue color depends on the EPF[1:0] setting.

6-bit data bus interface (D[5:0] is used) , DPI[2:0] = 110 , and RIM=1

	D5	D4	D3	D2	D1	D0	D5	D4	D3	D2	D1	D0	D5	D4	D3	D2	D1	D0
18bpp Frame Memory Write	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

6-bit data bus interface (D[5:0] is used) , DPI[2:0] = 101 , and RIM=1

	D5	D4	D3	D2	D1	D0	D5	D4	D3	D2	D1	D0	D5	D4	D3	D2	D1	D0
16bpp Frame Memory Write	R[4]	R[3]	R[2]	R[1]	R[0]		G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	

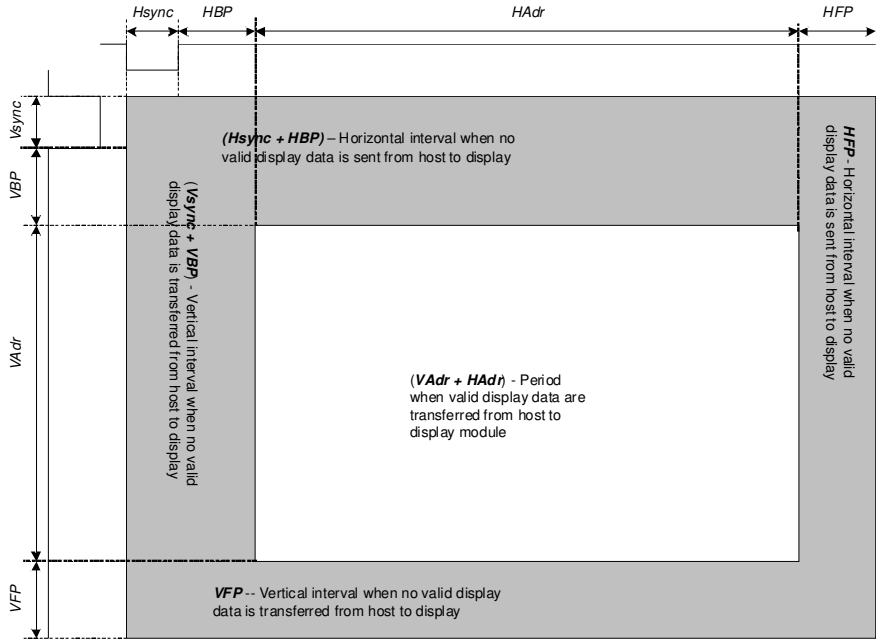
The LSB data of red/blue color depends on the EPF[1:0] setting.

Pixel clock (DOTCLK) is running all the time without stopping and used to enter VSYNC, HSYNC, DE and D [17:0] states when there is a rising edge of the DOTCLK. The DOTCLK cannot be used as continues internal

clock for other functions of the display module. Vertical synchronization (VSYNC) is used to tell when there is received a new frame of the display. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.

Horizontal synchronization (HSYNC) is used to tell when there is received a new line of the frame. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.

In DE mode, Data Enable (DE) is used to tell when there is received RGB information that should be transferred on the display. This is a high enable and its state is read to the display module by a rising edge of the DOTCLK signal. D [17:0] are used to tell what is the information of the image that is transferred on the display (When DE= '0' (low) and there is a rising edge of DOTCLK). D [17:0] can be '0' (low) or '1' (high). These lines are read by a rising edge of the DOTCLK signal. In SYNC mode, the valid display data in inputted in pixel unit via D [17:0] according to HFP/HBP settings of HSYNC signal and VFP/VBP setting of VSYNC. In both RGB interface modes, the input display data is written to GRAM first then outputs corresponding source voltage according the gray data from GRAM.



Parameters	Symbols	Condition	Min.	Typ.	Max.	Units
Horizontal Synchronization	Hsync		2	10	16	DOTCLK
Horizontal Back Porch	HBP		2	20	24	DOTCLK
Horizontal Back Porch(By pass mode)*	HBP(BP)		58	64	200	DOTCLK
Horizontal Address	HAdr		-	240	-	DOTCLK
Horizontal Front Porch	HFP		2	10	16	DOTCLK
Vertical Synchronization	Vsync		1	2	4	Line
Vertical Back Porch	VBP		1	2	-	Line
Vertical Address	VAdr		-	320	-	Line
Vertical Front Porch	VFP		3	4	-	Line

Note1: HBP setting need to 3 times in RGB 6/6/6 by pass mode. It can set HBP[0:8] in RB5h.

Typical values are setting example when used with panel resolution 240 x 320 (QVGA), clock frequency 6.35MHz and frame frequency about 70Hz.

Notes:

1. Vertical period (one frame) shall be equal to the sum of Vsync + VBP + VAdr + VFP.
2. Horizontal period (one line) shall be equal to the sum of Hsync + HBP + HAdr + HFP.
3. Control signals PCLK and Hsync shall be transmitted as specified at all times while valid pixels are transferred between the host processor and the display module.

Also make sure that

(Number of PCLK per 1 line) ≥ (Number of RTN clock) x Division ratio (DIV) x PCDIV

Setting Example for Display Control Clock in RGB Interface Operation

Register Display operation using DPI is in synchronization with internal clock PCLKD which is generated by dividing DOTCLK.

PCDIV [5:0]: Number of DOTCLK during internal clock PCLKD's high / low period. In units of 1 clock.

PCDIV specifying DOTCLK's division ratio, are determined so that difference between PCLKD's frequency and internal oscillation clock 615KHz is the smallest. Set PCDIV follow the restriction

(Number of PCLK in 1H) ≥ (Number of RTN clock) x Division ratio (DIV) x PCDIV.

Setting Example: To set frame frequency to 70Hz:

Internal Clock

Internal Oscillation Clock: 615KHz

DIV[1:0] = 2'b0 (x 1/1)

RTN[4:0] = 5'h1b (27 clocks)

FP = 7'h2 (2 lines), BP = 7'h2 (2 lines), NL = 6'h27 (320 lines)

Frame Rate → 70.30Hz

DOTCLK

HSYNC = 10 CLK

HBP = 20 CLK

HFP=10 CLK

70Hz x (2 + 320 + 2) lines x (10 + 20 + 240 + 10) clocks = 6.35MHz

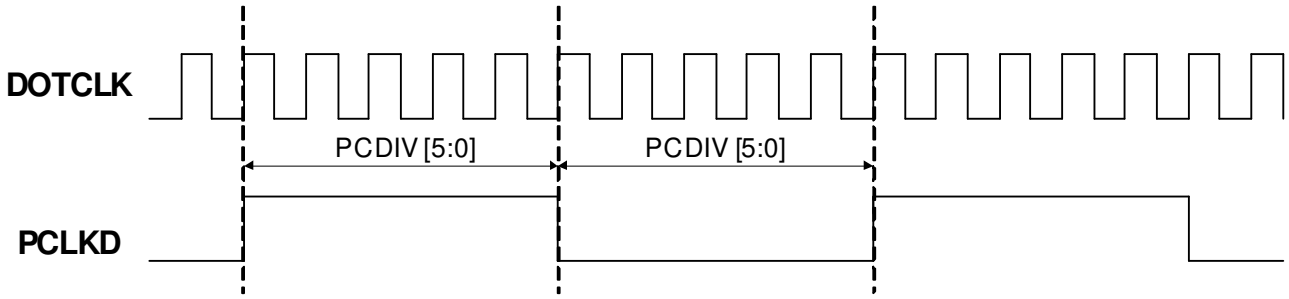
DOTCLK frequency = 6.35MHz

6.35 MHz / 615KHz = 10.32 Set PCDIV so that PCLK is divided by 10.

external fosc = 6.35 MHz / 10 = 635KHz

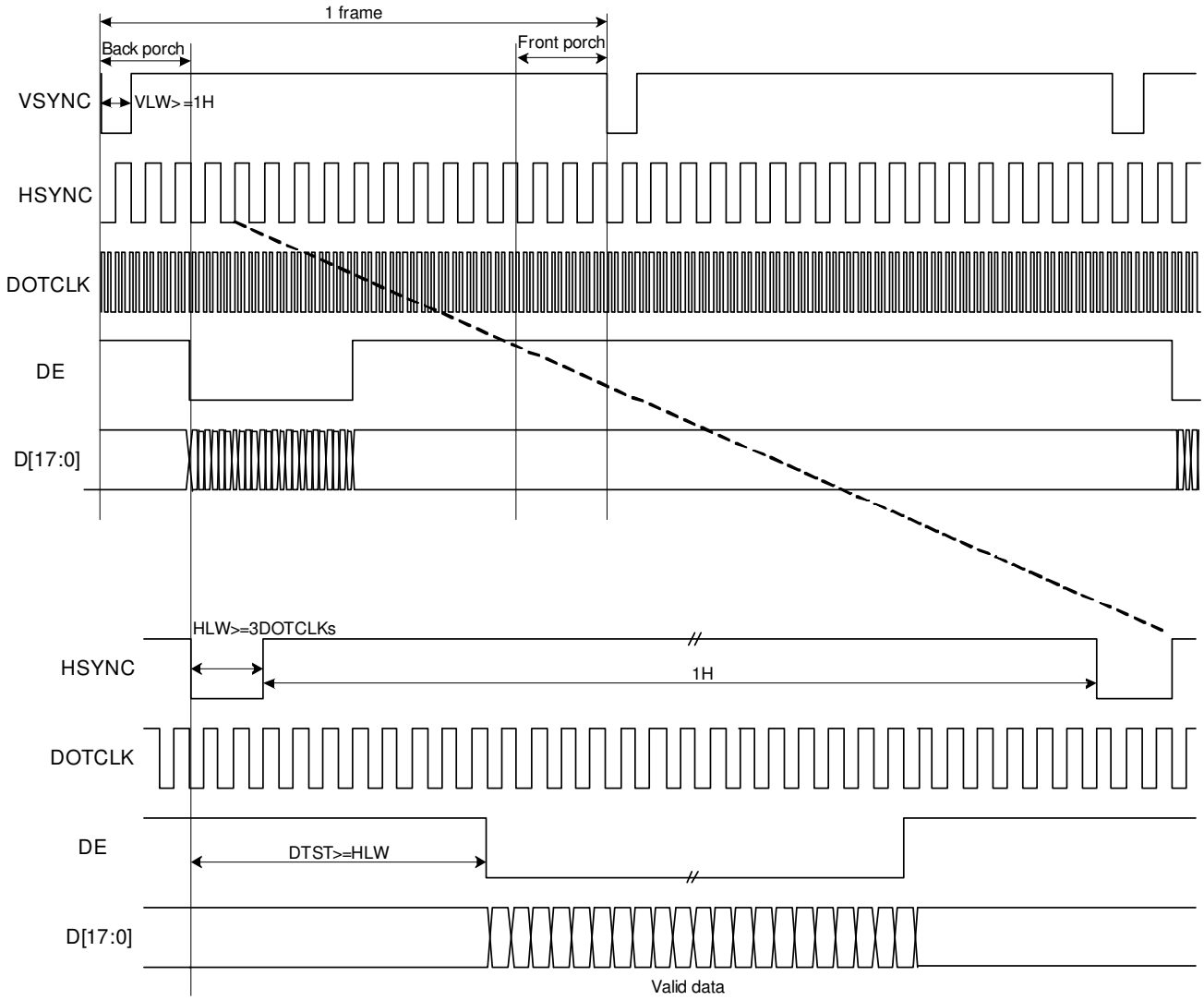
PCDIV = [6.35MHz / 635KHz) / 2] - 1 = 4

PCDIV[5:0] = 6'h04 (10 DOTCLK)



7.2.2. RGB Interface Timing

The timing chart of 18-/16-bit RGB interface mode is shown as below.

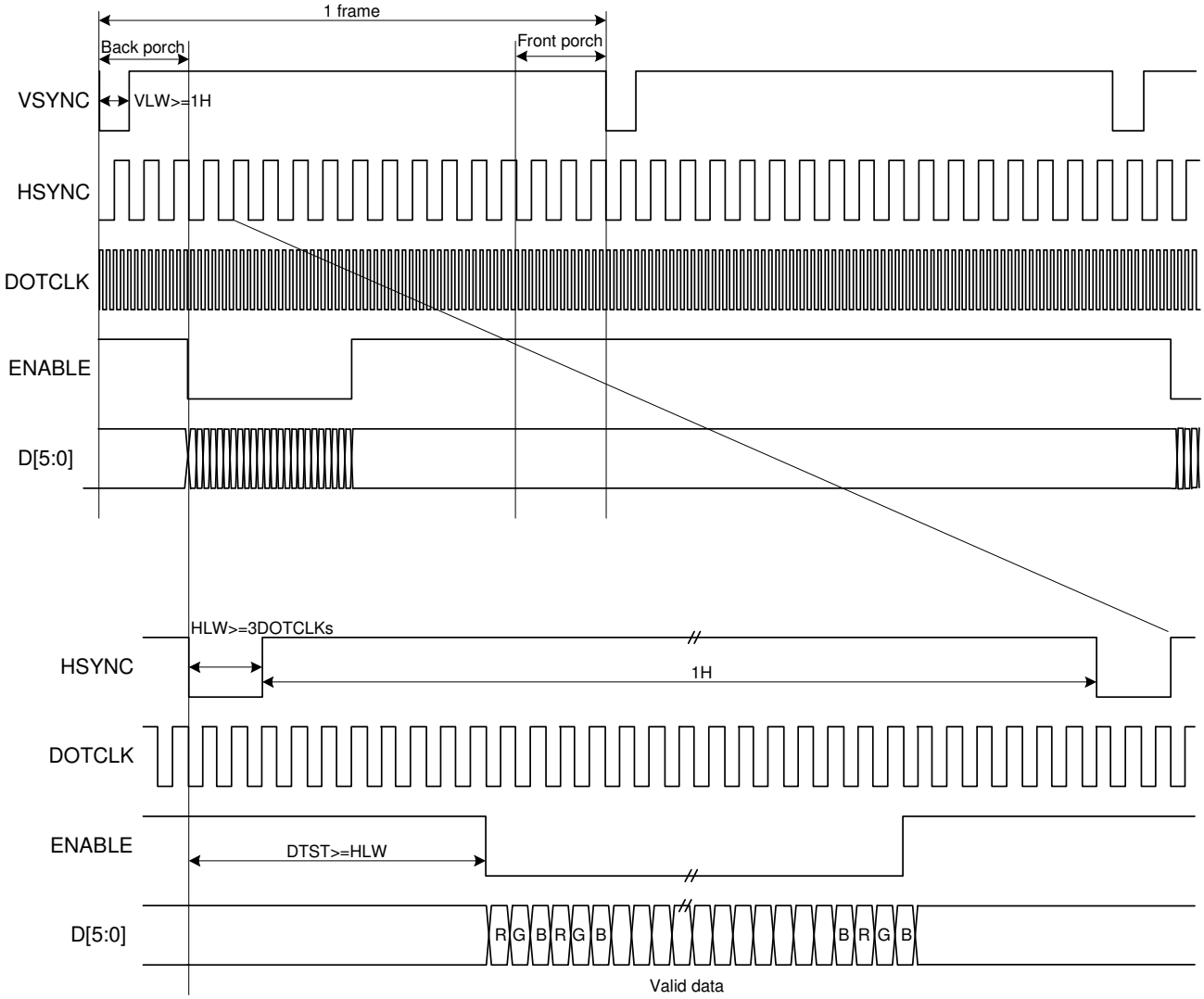


VLW : VSYNC Low Width
HLW : HSYNC Low Width
DTST : Data Transfer Startup Time

Note 1: The DE signal is not needed when RGB interface SYNC mode is selected.

Note 2: VSPL='0', HSPL='0', DPL='0' and EPL='1' of "Interface Mode Control (B0h)" command.

The timing chart of 6-bit RGB interface mode is shown as below:



VLW : VSYNC Low Width
HLW : HSYNC Low Width
DTST : Data Transfer Startup Time

Note 1: The DE signal is not needed when RGB interface SYNC mode is selected.

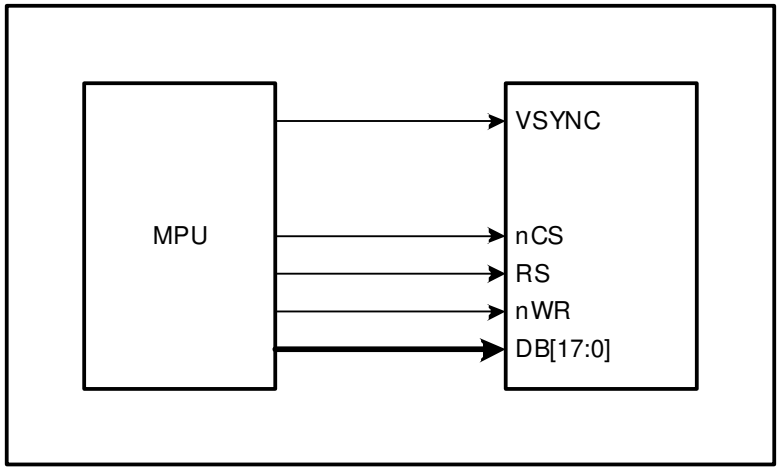
Note 2: VSPL='0', HSPL='0', DPL='0' and EPL='1' of "Interface Mode Control (B0h)" command.

Note 3: In 6-bit RGB interface mode, each dot of one pixel (R, G and B) is transferred in synchronization with DOTCLK.

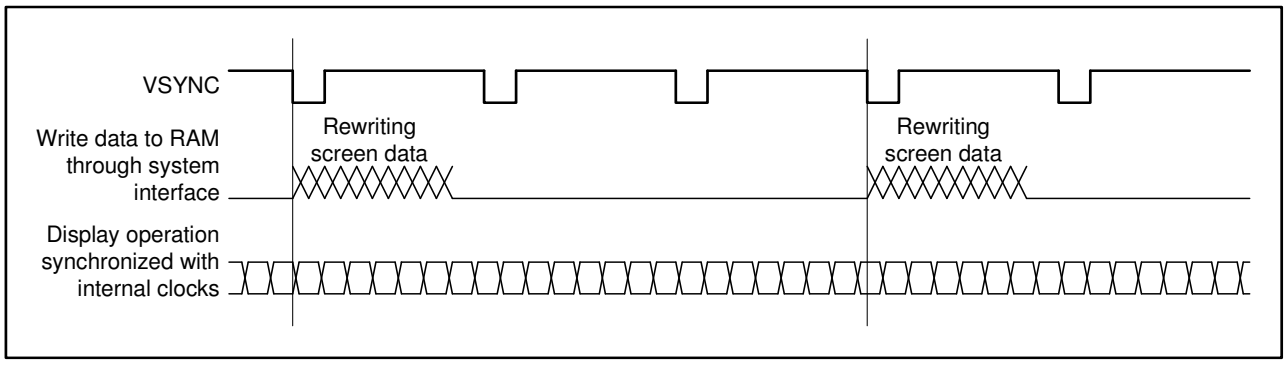
Note 4: In 6-bit RGB interface mode, set the cycles of VSYNC, HSYNC and DE to 3 multiples of DOTCLK.

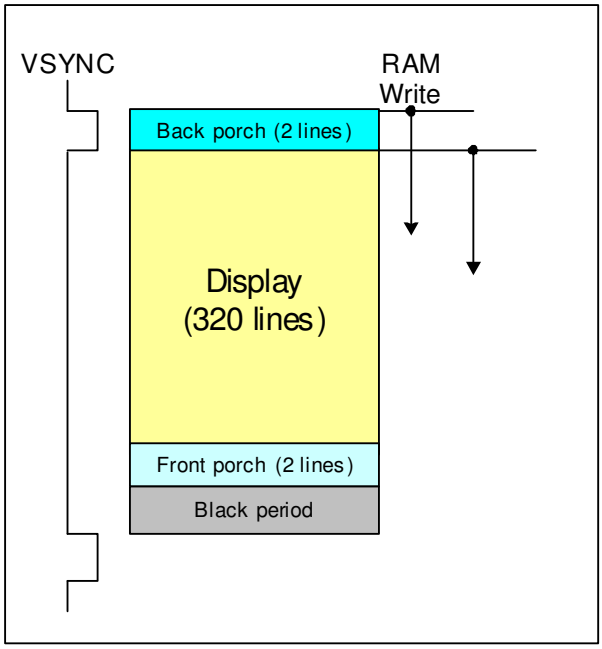
7.3. VSYNC Interface

ILI9340 supports the VSYNC interface in synchronization with the frame-synchronizing signal VSYNC to display the moving picture with the 8080-Ⅰ/8080-Ⅱ system interface. When the VSYNC interface is selected to display a moving picture, the minimum GRAM update speed is limited and the VSYNC interface is enabled by setting DM[1:0] = “10” and RM = “0”.



In the VSYNC mode, the display operation is synchronized with the internal clock and VSYNC input and the frame rate is determined by the pulse rate of VSYNC signal. All display data are stored in GRAM to minimize total data transfer required for moving picture display.





The VSYNC interface has the minimum speed limitation of writing data to the internal GRAM via the system interface, which are calculated from the following formula.

Internal clock frequency (fosc.) [Hz] = FrameFrequency x (DisplayLine (NL) + FrontPorch (VFP) + BackPorch (VBP)) x ClockCyclePerLines (RTN) x FrequencyFluctuation.

$$\textit{Minimum RAM write speed [Hz]} > \frac{240 \times DisplayLines(NL)}{[BackPorch(VBP) + DisplayLines(NL) - margins] \times Clocks\ per\ line \times (1/fosc)}$$

Note: When the RAM write operation does not start from the falling edge of VSYNC, the time from the falling edge of VSYNC until the start of RAM write operation must also be taken into account.

An example of minimum GRAM writing speed and internal clock frequency in VSYNC interface mode is as below.

[Example]

Display size: 240 RGB × 320 lines

Lines: 320 lines (NL = 100111)

Back porch: 2 lines (VBP = 0000010)

Front porch: 2 lines (VFP = 0000010)

Frame frequency: 70 Hz

Frequency fluctuation: 10%

Internal oscillator clock (fosc.) [Hz] = 70 x [320+ 2 + 2] x 27 clocks x (1.1/0.9) ≒ 748KHz

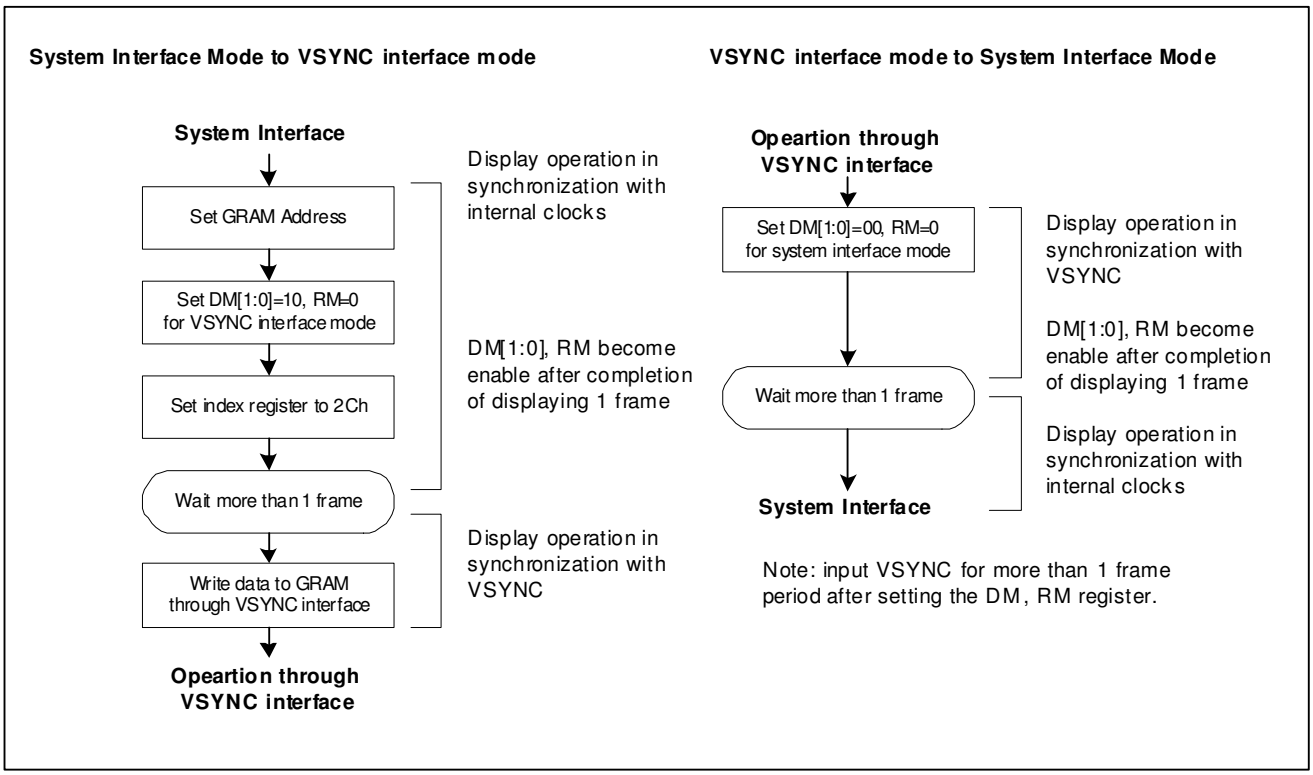
When calculate the internal clock frequency, the oscillator variation is needed to be taken into consideration. In the above example, the calculated internal clock frequency with ±10% margin variation is considered and ensures to complete the display operation within one VSYNC cycle. The causes of frequency variation come from fabrication process of LSI, room temperature, external resistors and VCI voltage variation.

Minimum speed for RAM writing [Hz] > 240 x 320 x 748K / [(2 + 320 – 2)lines x 27clocks] ≒ 6.65 MHz

The above theoretical value is calculated based on the premise that the ILI9340 starts to write data into the internal GRAM on the falling edge of VSYNC. There must at least be a margin of 2 lines between the physical display line and the GRAM line address where data writing operation is performed. The GRAM write speed of 6.65MHz or more will guarantee the completion of GRAM write operation before the ILI9340 starts to display the GRAM data on the screen and enable to rewrite the entire screen without flicker.

Notes in using the VSYNC interface

1. The minimum GRAM write speed must be satisfied and the frequency variation must be taken into consideration.
2. The display frame rate is determined by the VSYNC signal and the period of VSYNC must be longer than the scan period of an entire display.
3. When switching from the internal clock operation mode (DM[1:0] = “00”) to the VSYNC interface mode or inversely, the switching starts from the next VSYNC cycle, i.e. after completing the display of the frame.
4. The partial display, vertical scroll, and interlaced scan functions are not available in VSYNC interface mode.



7.4. Color Depth Conversion Look Up Table

When ILI9340 operates in parallel 16-bit interface, the color depth conversion is done by look-up table and extend input data format to 18-bit. See the detailed for look-up table of color depth conversion.

R input (5-bit) 16-bit/pixel –mode 65,536 colors	R output (6-bit) 18-bit/pixel –mode 262,144 colors	Command Code (0x2Dh) RGBSET Parameter
00000	R_{005} R_{004} R_{003} R_{002} R_{001} R_{000}	1
00001	R_{015} R_{014} R_{013} R_{012} R_{011} R_{010}	2
00010	R_{025} R_{024} R_{023} R_{022} R_{021} R_{020}	3
00011	R_{035} R_{034} R_{033} R_{032} R_{031} R_{030}	4
00100	R_{045} R_{044} R_{043} R_{042} R_{041} R_{040}	5
00101	R_{055} R_{054} R_{053} R_{052} R_{051} R_{050}	6
00110	R_{065} R_{064} R_{063} R_{062} R_{061} R_{060}	7
00111	R_{075} R_{074} R_{073} R_{072} R_{071} R_{070}	8
01000	R_{085} R_{084} R_{083} R_{082} R_{081} R_{080}	9
01001	R_{095} R_{094} R_{093} R_{092} R_{091} R_{090}	10
01010	R_{105} R_{104} R_{103} R_{102} R_{101} R_{100}	11
01011	R_{115} R_{114} R_{113} R_{112} R_{111} R_{110}	12
01100	R_{125} R_{124} R_{123} R_{122} R_{121} R_{120}	13
01101	R_{135} R_{134} R_{133} R_{132} R_{131} R_{130}	14
01110	R_{145} R_{144} R_{143} R_{142} R_{141} R_{140}	15
01111	R_{155} R_{154} R_{153} R_{152} R_{151} R_{150}	16
10000	R_{165} R_{164} R_{163} R_{162} R_{161} R_{160}	17
10001	R_{175} R_{174} R_{173} R_{172} R_{171} R_{170}	18
10010	R_{185} R_{184} R_{183} R_{182} R_{181} R_{180}	19
10011	R_{195} R_{194} R_{193} R_{192} R_{191} R_{190}	20
10100	R_{205} R_{204} R_{203} R_{202} R_{201} R_{200}	21
10101	R_{215} R_{214} R_{213} R_{212} R_{211} R_{210}	22
10110	R_{225} R_{224} R_{223} R_{222} R_{221} R_{220}	23
10111	R_{235} R_{234} R_{233} R_{232} R_{231} R_{230}	24
11000	R_{245} R_{244} R_{243} R_{242} R_{241} R_{240}	25
11001	R_{255} R_{254} R_{253} R_{252} R_{251} R_{250}	26
11010	R_{265} R_{264} R_{263} R_{262} R_{261} R_{260}	27
11011	R_{275} R_{274} R_{273} R_{272} R_{271} R_{270}	28
11100	R_{285} R_{284} R_{283} R_{282} R_{281} R_{280}	29
11101	R_{295} R_{294} R_{293} R_{292} R_{291} R_{290}	30
11110	R_{305} R_{304} R_{303} R_{302} R_{301} R_{300}	31
11111	R_{315} R_{314} R_{313} R_{312} R_{311} R_{310}	32

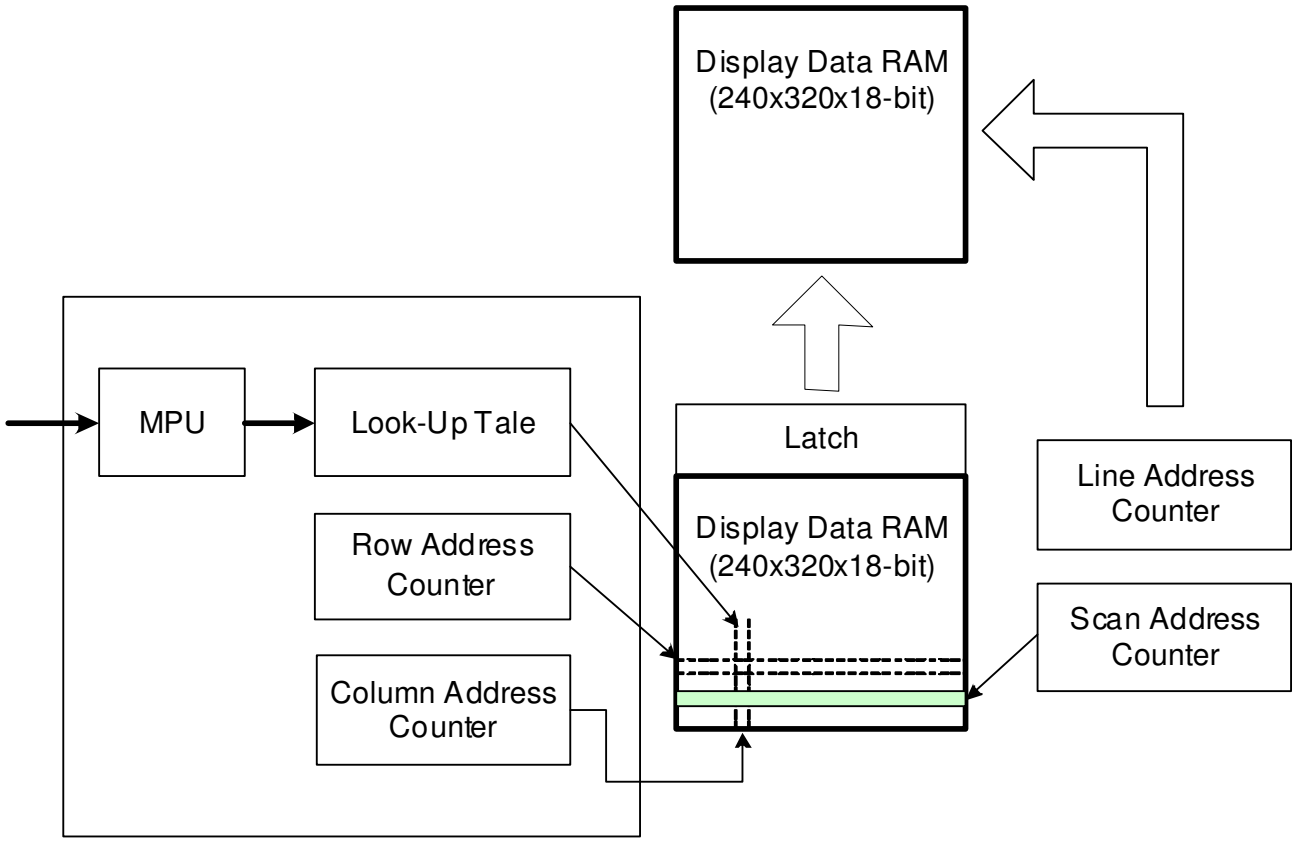
G input (6-bit) 16-bit/pixel –mode 65,536 colors	G output (6-bit) 18-bit/pixel –mode 262,144 colors	Command Code (0x2Dh) RGBSET Parameter
000000	G_{005} G_{004} G_{003} G_{002} G_{001} G_{000}	33
000001	G_{015} G_{014} G_{013} G_{012} G_{011} G_{010}	34
000010	G_{025} G_{024} G_{023} G_{022} G_{021} G_{020}	35
000011	G_{035} G_{034} G_{033} G_{032} G_{031} G_{030}	36
000100	G_{045} G_{044} G_{043} G_{042} G_{041} G_{040}	37
000101	G_{055} G_{054} G_{053} G_{052} G_{051} G_{050}	38
000110	G_{065} G_{064} G_{063} G_{062} G_{061} G_{060}	39
000111	G_{075} G_{074} G_{073} G_{072} G_{071} G_{070}	40
001000	G_{085} G_{084} G_{083} G_{082} G_{081} G_{080}	41
001001	G_{095} G_{094} G_{093} G_{092} G_{091} G_{090}	42
001010	G_{105} G_{104} G_{103} G_{102} G_{101} G_{100}	43
001011	G_{115} G_{114} G_{113} G_{112} G_{111} G_{110}	44
001100	G_{125} G_{124} G_{123} G_{122} G_{121} G_{120}	45
001101	G_{135} G_{134} G_{133} G_{132} G_{131} G_{130}	46
001110	G_{145} G_{144} G_{143} G_{142} G_{141} G_{140}	47
001111	G_{155} G_{154} G_{153} G_{152} G_{151} G_{150}	48
010000	G_{165} G_{164} G_{163} G_{162} G_{161} G_{160}	49
010001	G_{175} G_{174} G_{173} G_{172} G_{171} G_{170}	50
010010	G_{185} G_{184} G_{183} G_{182} G_{181} G_{180}	51
010011	G_{195} G_{194} G_{193} G_{192} G_{191} G_{190}	52
010100	G_{205} G_{204} G_{203} G_{202} G_{201} G_{200}	53
010101	G_{215} G_{214} G_{213} G_{212} G_{211} G_{210}	54
010110	G_{225} G_{224} G_{223} G_{222} G_{221} G_{220}	55
010111	G_{235} G_{234} G_{233} G_{232} G_{231} G_{230}	56
011000	G_{245} G_{244} G_{243} G_{242} G_{241} G_{240}	57
011001	G_{255} G_{254} G_{253} G_{252} G_{251} G_{250}	58
011010	G_{265} G_{264} G_{263} G_{262} G_{261} G_{260}	59
011011	G_{275} G_{274} G_{273} G_{272} G_{271} G_{270}	60
011100	G_{285} G_{284} G_{283} G_{282} G_{281} G_{280}	61
011101	G_{295} G_{294} G_{293} G_{292} G_{291} G_{290}	62
011110	G_{305} G_{304} G_{303} G_{302} G_{301} G_{300}	63
011111	G_{315} G_{314} G_{313} G_{312} G_{311} G_{310}	64
100000	G_{325} G_{324} G_{323} G_{322} G_{321} G_{320}	65
100001	G_{335} G_{334} G_{333} G_{332} G_{331} G_{330}	66

G input (6-bit) 16-bit/pixel –mode 65,536 colors	G output (6-bit) 18-bit/pixel –mode 262,144 colors	Command Code (0x2Dh) RGBSET Parameter
100010	G_{345} G_{344} G_{343} G_{342} G_{341} G_{340}	67
100011	G_{355} G_{354} G_{353} G_{352} G_{351} G_{350}	68
100100	G_{365} G_{364} G_{363} G_{362} G_{361} G_{360}	69
100101	G_{375} G_{374} G_{373} G_{372} G_{371} G_{370}	70
100110	G_{385} G_{384} G_{383} G_{382} G_{381} G_{380}	71
100111	G_{395} G_{394} G_{393} G_{392} G_{391} G_{390}	72
101000	G_{405} G_{404} G_{403} G_{402} G_{401} G_{400}	73
101001	G_{415} G_{414} G_{413} G_{412} G_{411} G_{410}	74
101010	G_{425} G_{424} G_{423} G_{422} G_{421} G_{420}	75
101011	G_{435} G_{434} G_{433} G_{432} G_{431} G_{430}	76
101100	G_{445} G_{444} G_{443} G_{442} G_{441} G_{440}	77
101101	G_{455} G_{454} G_{453} G_{452} G_{451} G_{450}	78
101110	G_{465} G_{464} G_{463} G_{462} G_{461} G_{460}	79
101111	G_{475} G_{474} G_{473} G_{472} G_{471} G_{470}	80
110000	G_{485} G_{484} G_{483} G_{482} G_{481} G_{480}	81
110001	G_{495} G_{494} G_{493} G_{492} G_{491} G_{490}	82
110010	G_{505} G_{504} G_{503} G_{502} G_{501} G_{500}	83
110011	G_{515} G_{514} G_{513} G_{512} G_{511} G_{510}	84
110100	G_{525} G_{524} G_{523} G_{522} G_{521} G_{520}	85
110101	G_{535} G_{534} G_{533} G_{532} G_{531} G_{530}	86
110110	G_{545} G_{544} G_{543} G_{542} G_{541} G_{540}	87
110111	G_{555} G_{554} G_{553} G_{552} G_{551} G_{550}	88
111000	G_{565} G_{564} G_{563} G_{562} G_{561} G_{560}	89
111001	G_{575} G_{574} G_{573} G_{572} G_{571} G_{570}	90
111010	G_{585} G_{584} G_{583} G_{582} G_{581} G_{580}	91
111011	G_{595} G_{594} G_{593} G_{592} G_{591} G_{590}	92
111100	G_{605} G_{604} G_{603} G_{602} G_{601} G_{600}	93
111101	G_{615} G_{614} G_{613} G_{612} G_{611} G_{610}	94
111110	G_{625} G_{624} G_{623} G_{622} G_{621} G_{620}	95
111111	G_{635} G_{634} G_{633} G_{632} G_{631} G_{630}	96

B input (5-bit) 16-bit/pixel –mode 65,536 colors	B output (6-bit) 18-bit/pixel –mode 262,144 colors	Command Code (0x2Dh) RGBSET Parameter
00000	B_{005} B_{004} B_{003} B_{002} B_{001} B_{000}	97
00001	B_{015} B_{014} B_{013} B_{012} B_{011} B_{010}	98
00010	B_{025} B_{024} B_{023} B_{022} B_{021} B_{020}	99
00011	B_{035} B_{034} B_{033} B_{032} B_{031} B_{030}	100
00100	B_{045} B_{044} B_{043} B_{042} B_{041} B_{040}	101
00101	B_{055} B_{054} B_{053} B_{052} B_{051} B_{050}	102
00110	B_{065} B_{064} B_{063} B_{062} B_{061} B_{060}	103
00111	B_{075} B_{074} B_{073} B_{072} B_{071} B_{070}	104
01000	B_{085} B_{084} B_{083} B_{082} B_{081} B_{080}	105
01001	B_{095} B_{094} B_{093} B_{092} B_{091} B_{090}	106
01010	B_{105} B_{104} B_{103} B_{102} B_{101} B_{100}	107
01011	B_{115} B_{114} B_{113} B_{112} B_{111} B_{110}	108
01100	B_{125} B_{124} B_{123} B_{122} B_{121} B_{120}	109
01101	B_{135} B_{134} B_{133} B_{132} B_{131} B_{130}	110
01110	B_{145} B_{144} B_{143} B_{142} B_{141} B_{140}	111
01111	B_{155} B_{154} B_{153} B_{152} B_{151} B_{150}	112
10000	B_{165} B_{164} B_{163} B_{162} B_{161} B_{160}	113
10001	B_{175} B_{174} B_{173} B_{172} B_{171} B_{170}	114
10010	B_{185} B_{184} B_{183} B_{182} B_{181} B_{180}	115
10011	B_{195} B_{194} B_{193} B_{192} B_{191} B_{190}	116
10100	B_{205} B_{204} B_{203} B_{202} B_{201} B_{200}	117
10101	B_{215} B_{214} B_{213} B_{212} B_{211} B_{210}	118
10110	B_{225} B_{224} B_{223} B_{222} B_{221} B_{220}	119
10111	B_{235} B_{234} B_{233} B_{232} B_{231} B_{230}	120
11000	B_{245} B_{244} B_{243} B_{242} B_{241} B_{240}	121
11001	B_{255} B_{254} B_{253} B_{252} B_{251} B_{250}	122
11010	B_{265} B_{264} B_{263} B_{262} B_{261} B_{260}	123
11011	B_{275} B_{274} B_{273} B_{272} B_{271} B_{270}	124
11100	B_{285} B_{284} B_{283} B_{282} B_{281} B_{280}	125
11101	B_{295} B_{294} B_{293} B_{292} B_{291} B_{290}	126
11110	B_{305} B_{304} B_{303} B_{302} B_{301} B_{300}	127
11111	B_{315} B_{314} B_{313} B_{312} B_{311} B_{310}	128

7.5. Display Data RAM (DDRAM)

ILI9340 has an integrated 240x320x18-bit graphic type static RAM. This 172,800-byte memory allows storing a 240xRGBx320 image with an 18-bit resolution (262K-color). There is no abnormal visible effect on the display when there are simultaneous panel display read and interface read/write to the same location of the frame memory.

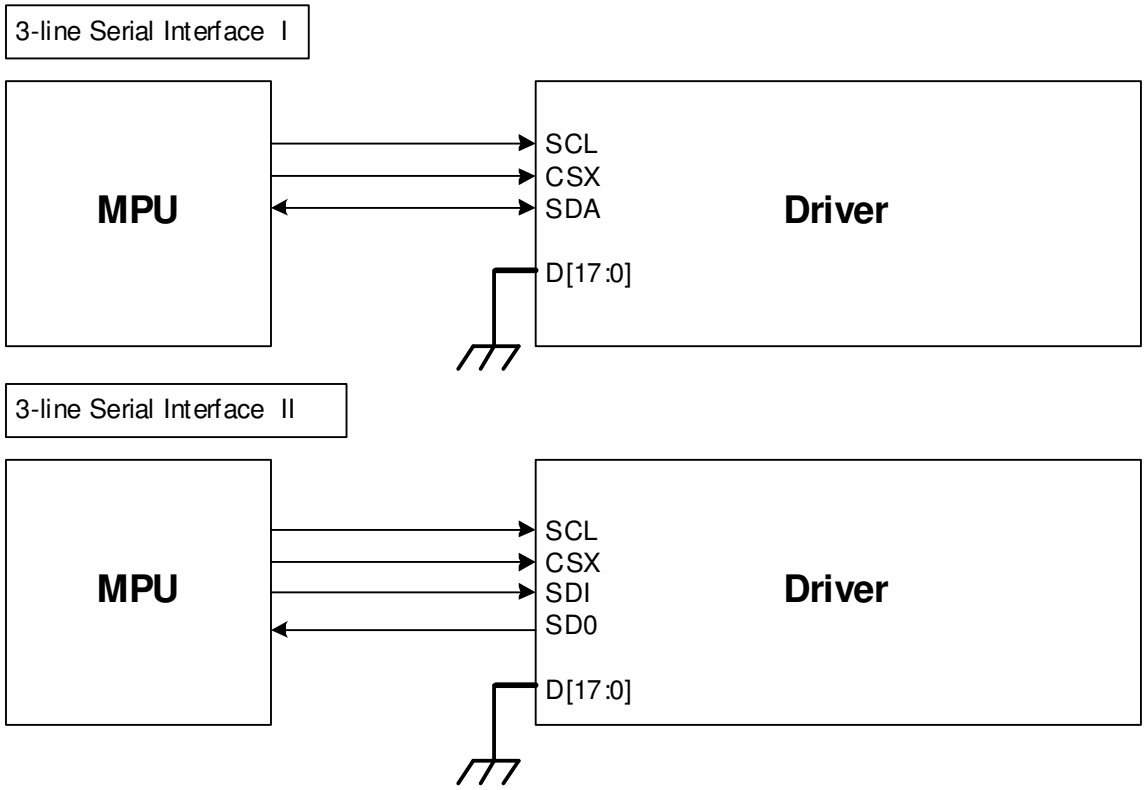


7.6. Display Data Format

ILI9340 supplies 18-/16-/9-/8-bit parallel MCU interface with 8080-Ⅰ/8080-Ⅱ series, 3-/4-line serial interface and 6-/16-18-bit parallel RGB interface. The parallel MCU interface and serial interface mode can be selected by external pins IM [3:0] and RGB interface mode can be selected by software command parameters RCM[1:0].

7.6.1. 3-line Serial Interface

The 3-line/9-bit serial bus interface of ILI9340 can be used by setting external pin as IM [3:0] to “0101” for serial interface I or IM [3:0] to “1101” for serial interface II. The shown figure is the example of 3-line SPI interface.

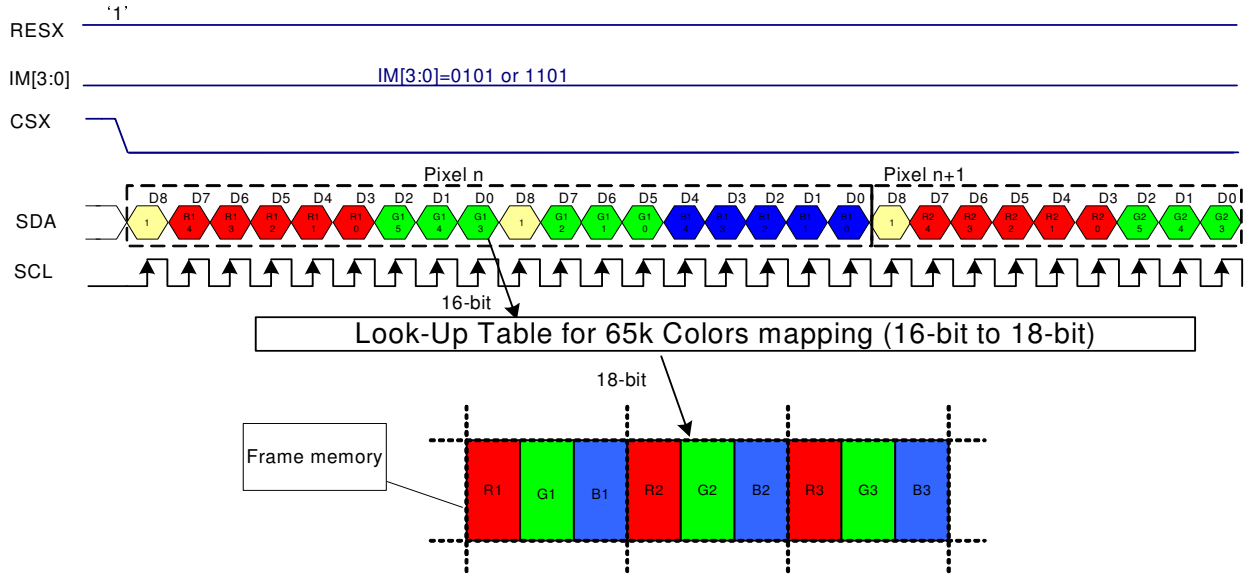


In 3-line serial interface, different display data format is available for two color depths supported by the LCM listed below.

-65k colors, RGB 5, 6, 5 -bits input

-262k colors, RGB 6, 6, 6 -bits input.

16 bit/pixel color order (R:5-bit, G:6-bit, B:5-bit), 65,536 colors



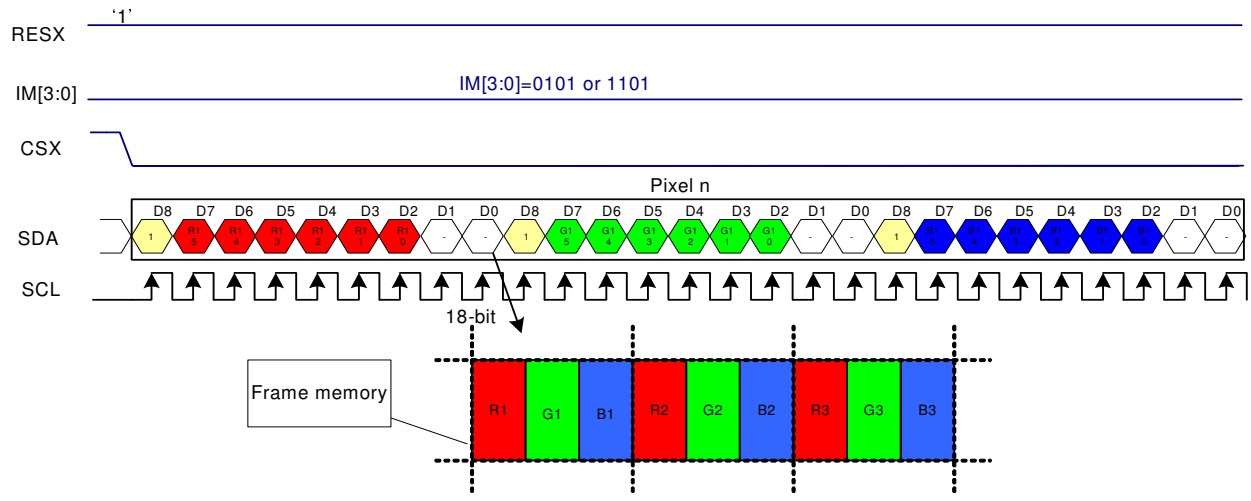
Note 1: The pixel data with 16-bit color depth information.

Note 2: The most significant bits are: Rx4, Gx5 and Bx4.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".

18 bit/pixel color order (R:6-bit, G:6-bit, B:6-bit), 262,144 colors



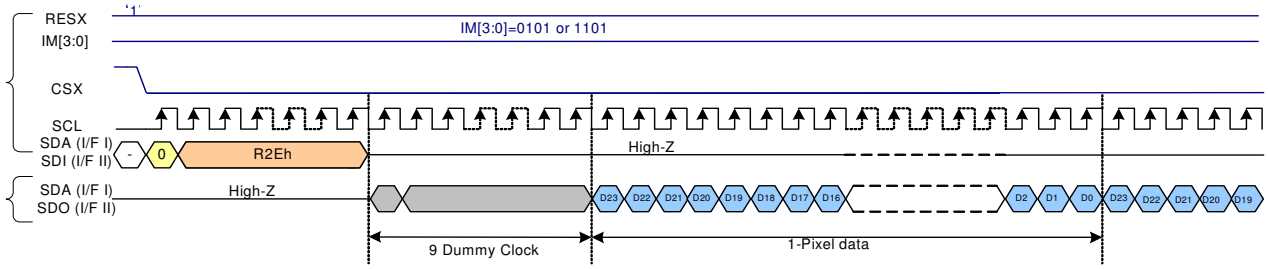
Note 1: The pixel data with 18-bit color depth information.

Note 2: The most significant bits are: Rx5, Gx5 and Bx5.

Note 3: The least significant bits are : Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care - Can be set "0" or "1".

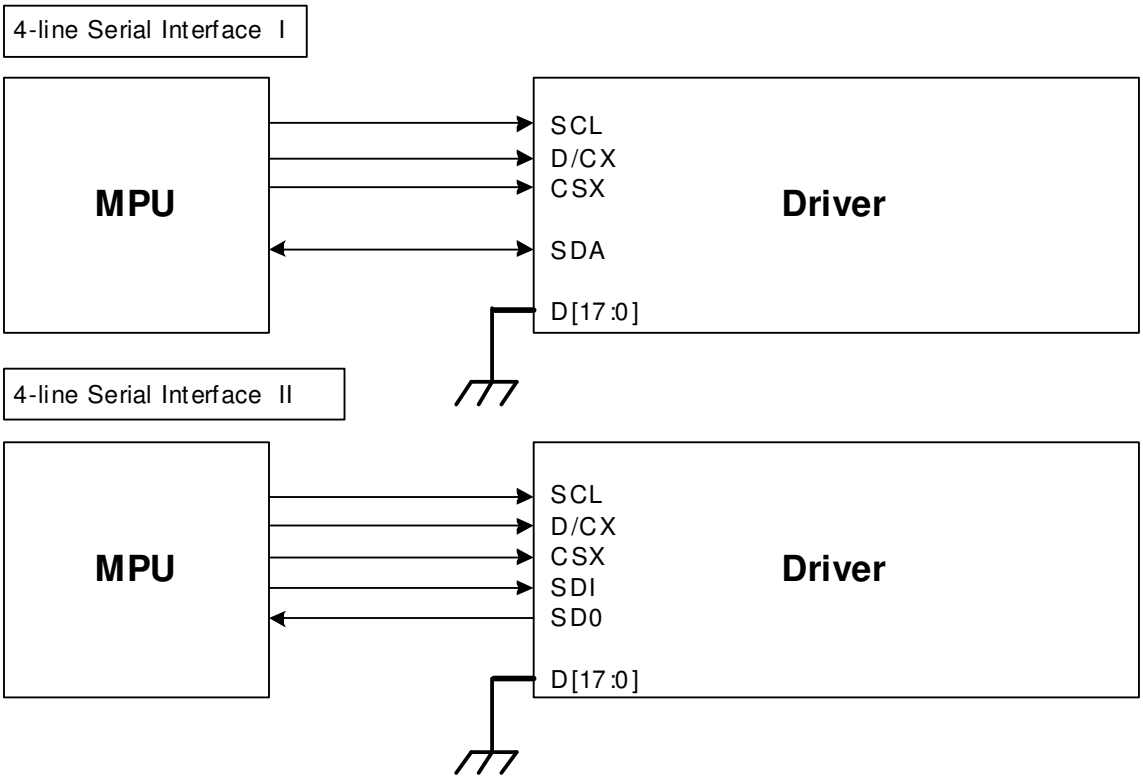
Read data through 3-line SPI mode



Note 1: '-'= Don't care –Can be set "0" or "1".

7.6.2. 4-line Serial Interface

The 4-line/8-bit serial bus interface of ILI9340 can be used by setting external pin as IM [3:0] to “0110” for serial interface I or IM [3:0] to “1110” for serial interface II. The shown figure is the example of 4-line SPI interface.

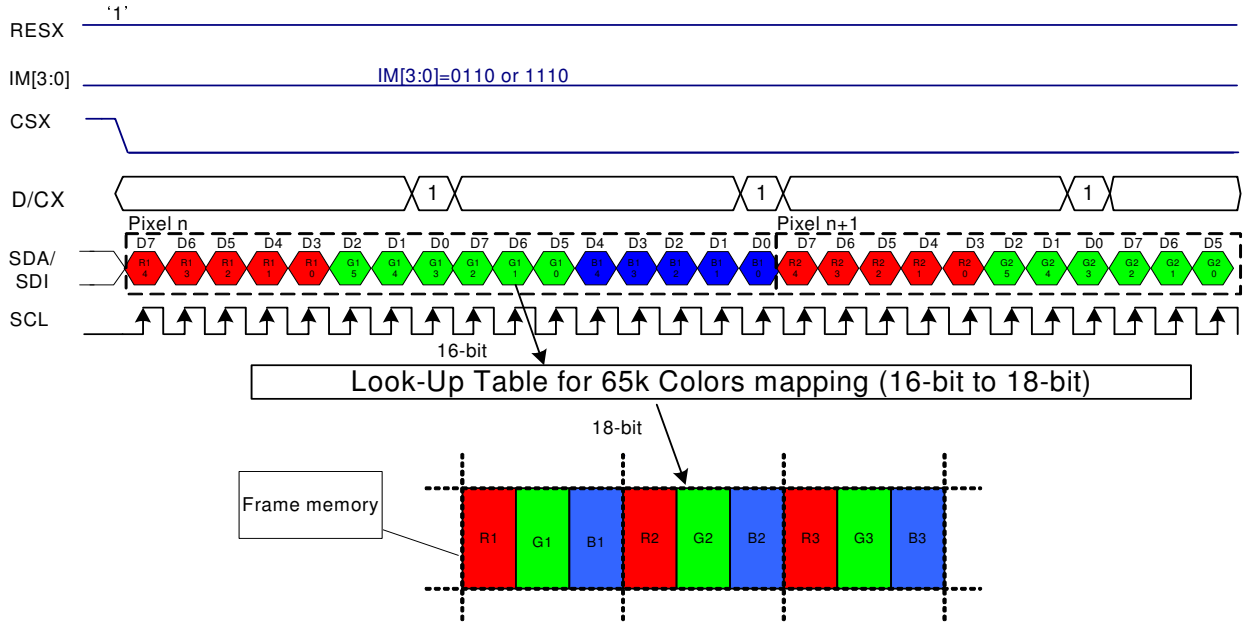


In 4-line serial interface, different display data format is available for two color depths supported by the LCM listed below.

-65k colors, RGB 5, 6, 5 -bits input.

-262k colors, RGB 6, 6, 6 -bits input.

16 bit/pixel color order (R:5-bit, G:6-bit, B:5-bit), 65,536 colors



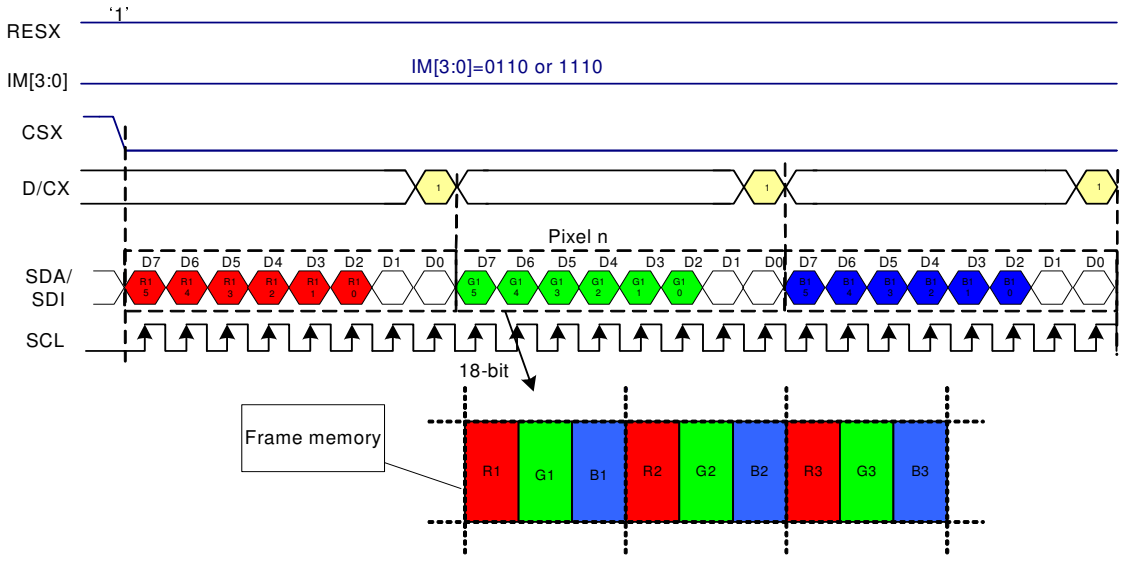
Note 1: The pixel data with 16-bit color depth information.

Note 2: The most significant bits are: Rx4, Gx5 and Bx4.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".

18 bit/pixel color order (R:6-bit, G:6-bit, B:6-bit), 262,144 colors



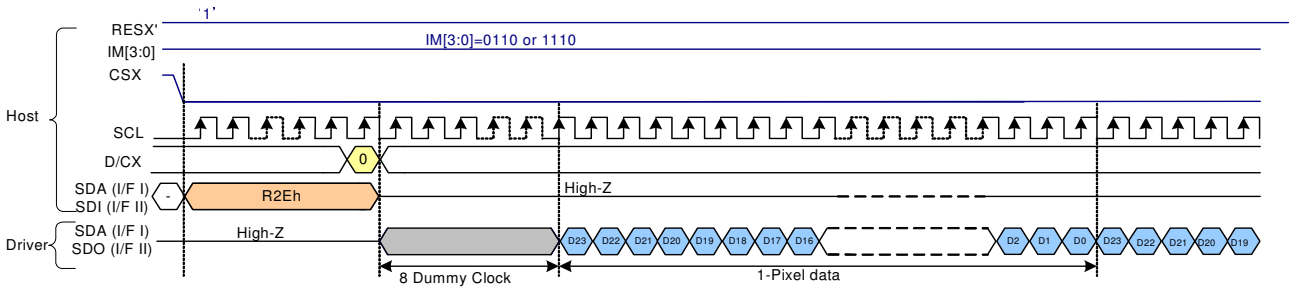
Note 1: The pixel data with 18-bit color depth information.

Note 2: The most significant bits are: Rx5, Gx5 and Bx5.

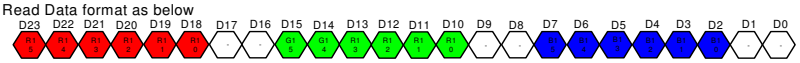
Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".

Read data through 4-line SPI mode



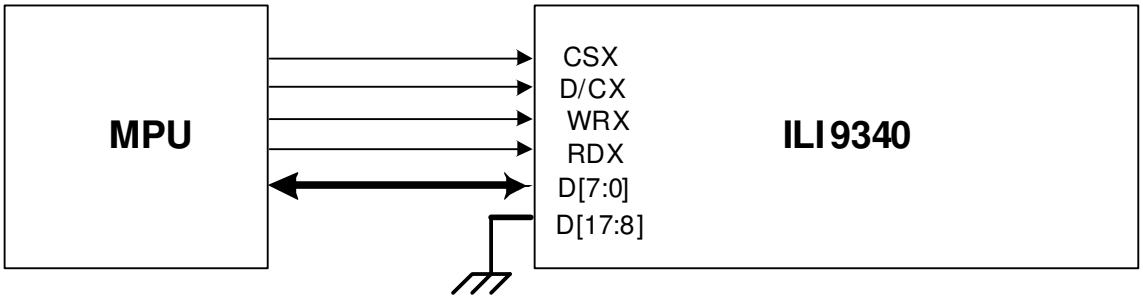
Read Data format as below



Note 1: '-'= Don't care – Can be set "0" or "1".

7.6.3. 8-bit Parallel MCU Interface

The 8080-Ⅰ system 8-bit parallel bus interface of ILI9340 can be used by setting external pin as IM [3:0] to "0000".The following shown figure is the example of interface with 8080-Ⅰ MCU system interface.



Different display data formats are available for two color depths supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 2 byte transfers when DBI [2:0] bits of 3Ah register are set to "101".

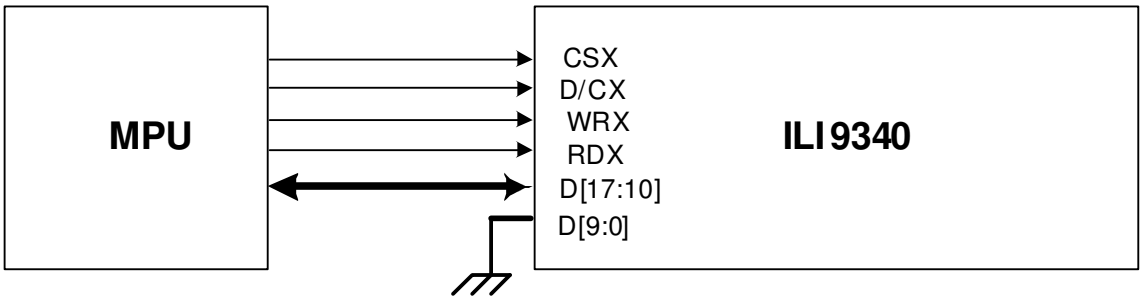
Count	0	1	2	3	4	…	477	478	479	480
D/CX	0	1	1	1	1	…	1	1	1	1
D7	C7	0R4	0G2	1R4	1G2	…	238R4	238G2	239R4	239G2
D6	C6	0R3	0G1	1R3	1G1	…	238R3	238G1	239R3	239G1
D5	C5	0R2	0G0	1R2	1G0	…	238R2	238G0	239R2	239G0
D4	C4	0R1	0B4	1R1	1B4	…	238R1	238B4	239R1	239B4
D3	C3	0R0	0B3	1R0	1B3	…	238R0	238B3	239R0	239B3
D2	C2	0G5	0B2	1G5	1B2	…	238G5	238B2	239G5	239B2
D1	C1	0G4	0B1	1G4	1B1	…	238G4	238B1	239G4	239B1
D0	C0	0G3	0B0	1G3	1B0	…	238G3	238B0	239G3	239B0

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when DBI [2:0] bits of 3Ah register are set to "110".

Count	0	1	2	3	…	718	719	720
D/CX	0	1	1	1	…	1	1	1
D7	C7	0R5	0G5	0B5	…	239R5	239G5	239B5
D6	C6	0R4	0G4	0B4	…	239R4	239G4	239B4
D5	C5	0R3	0G3	0B3	…	239R3	239G3	239B3
D4	C4	0R2	0G2	0B2	…	239R2	239G2	239B2
D3	C3	0R1	0G1	0B1	…	239R1	239G1	239B1
D2	C2	0R0	0G0	0B0	…	239R0	239G0	239B0
D1	C1				…			
D0	C0				…			

The 8080-Ⅱ system 8-bit parallel bus interface of ILI9340 can be used by settings as IM [3:0] ="1000". The following shown figure is the example of interface with 8080-Ⅱ MCU system interface.



Different display data formats are available for two color depths supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 2 byte transfers when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	4	…	477	478	479	480
D/CX	0	1	1	1	1	…	1	1	1	1
D17	C7	0R4	0G2	1R4	1G2	…	238R4	238G2	239R4	239G2
D16	C6	0R3	0G1	1R3	1G1	…	238R3	238G1	239R3	239G1
D15	C5	0R2	0G0	1R2	1G0	…	238R2	238G0	239R2	239G0
D14	C4	0R1	0B4	1R1	1B4	…	238R1	238B4	239R1	239B4
D13	C3	0R0	0B3	1R0	1B3	…	238R0	238B3	239R0	239B3
D12	C2	0G5	0B2	1G5	1B2	…	238G5	238B2	239G5	239B2
D11	C1	0G4	0B1	1G4	1B1	…	238G4	238B1	239G4	239B1
D10	C0	0G3	0B0	1G3	1B0	…	238G3	238B0	239G3	239B0

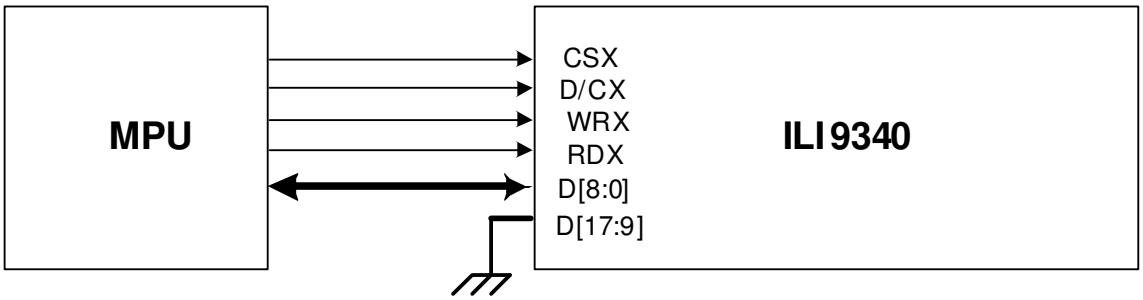
262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when DBI [2:0] bits of 3Ah register are set to "110".

Count	0	1	2	3	…	718	719	720
D/CX	0	1	1	1	…	1	1	1
D17	C7	0R5	0G5	0B5	…	239R5	239G5	239B5
D16	C6	0R4	0G4	0B4	…	239R4	239G4	239B4
D15	C5	0R3	0G3	0B3	…	239R3	239G3	239B3
D14	C4	0R2	0G2	0B2	…	239R2	239G2	239B2
D13	C3	0R1	0G1	0B1	…	239R1	239G1	239B1
D12	C2	0R0	0G0	0B0	…	239R0	239G0	239B0
D11	C1				…			
D10	C0				…			

7.6.4. 9-bit Parallel MCU Interface

The 8080-Ⅰ system 9-bit parallel bus interface of ILI9340 can be selected by setting hardware pin IM [3:0] to "0010". The following shown figure is the example of interface with 8080-Ⅰ MCU system interface.



65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 2 transfers when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	4	…	477	478	479	480
D/CX	0	1	1	1	1	…	1	1	1	1
D8										
D7	C7	0R4	0G2	1R4	1G2	…	238R4	238G2	239R4	239G2
D6	C6	0R3	0G1	1R3	1G1	…	238R3	238G1	239R3	239G1
D5	C5	0R2	0G0	1R2	1G0	…	238R2	238G0	239R2	239G0
D4	C4	0R1	0B4	1R1	1B4	…	238R1	238B4	239R1	239B4
D3	C3	0R0	0B3	1R0	1B3	…	238R0	238B3	239R0	239B3
D2	C2	0G5	0B2	1G5	1B2	…	238G5	238B2	239G5	239B2
D1	C1	0G4	0B1	1G4	1B1	…	238G4	238B1	239G4	239B1
D0	C0	0G3	0B0	1G3	1B0	…	238G3	238B0	239G3	239B0

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

There are 2 pixels (6 sub-pixels) display data is sent by 4 transfers, when DBI [2:0] bits of 3Ah register are set to "110".

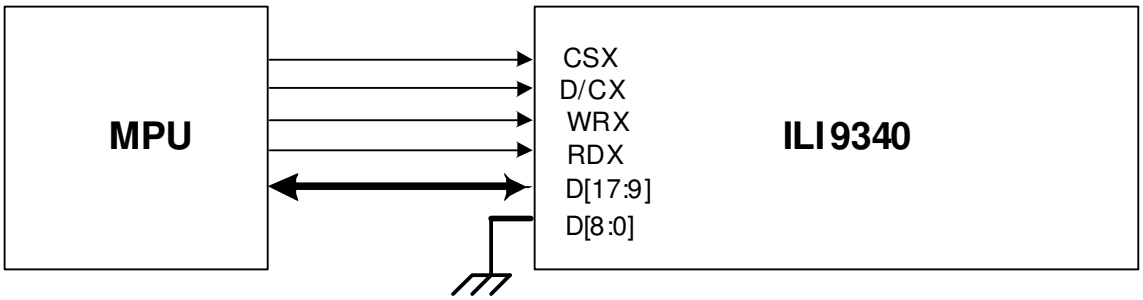
MDT[1:0]="00"

Count	0	1	2	3	4	…	478	478	479	480
D/CX	0	1	1	1	1	…	1	1	1	1
D8		0R5	0G2	1R5	1G2		238R5	238G2	239R5	239G2
D7	C7	0R4	0G1	1R4	1G1	…	238R4	238G1	239R4	239G1
D6	C6	0R3	0G0	1R3	1G0	…	238R3	238G0	239R3	239G0
D5	C5	0R2	0B5	1R2	1B5	…	238R2	238B5	239R2	239B5
D4	C4	0R1	0B4	1R1	1B4	…	238R1	238B4	239R1	239B4
D3	C3	0R0	0B3	1R0	1B3	…	238R0	238B3	239R0	239B3
D2	C2	0G5	0B2	1G5	1B2	…	238G5	238B2	239G5	239B2
D1	C1	0G4	0B1	1G4	1B1	…	238G4	238B1	239G4	239B1
D0	C0	0G3	0B0	1G3	1B0	…	238G3	238B0	239G3	239B0

MDT[1:0]="01"

Count	0	1	2	3	…	718	719	720
D/CX	0	1	1	1	…	1	1	1
D8								
D7	C7	0R5	0G5	0B5	…	239R5	239G5	239B5
D6	C6	0R4	0G4	0B4	…	239R4	239G4	239B4
D5	C5	0R3	0G3	0B3	…	239R3	239G3	239B3
D4	C4	0R2	0G2	0B2	…	239R2	239G2	239B2
D3	C3	0R1	0G1	0B1	…	239R1	239G1	239B1
D2	C2	0R0	0G0	0B0	…	239R0	239G0	239B0
D1	C1				…			
D0	C0				…			

The 8080-Ⅱ system 9-bit parallel bus interface of ILI9340 can be selected by setting hardware pin IM [3:0] to "1010". The following shown figure is the example of interface with 8080-Ⅱ MCU system interface.



65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 2 transfers when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	4	…	477	478	479	480
D/CX	0	1	1	1	1	…	1	1	1	1
D17	C7									
D16	C6	0R4	0G2	1R4	1G2	…	238R4	238G2	239R4	239G2
D15	C5	0R3	0G1	1R3	1G1	…	238R3	238G1	239R3	239G1
D14	C4	0R2	0G0	1R2	1G0	…	238R2	238G0	239R2	239G0
D13	C3	0R1	0B4	1R1	1B4	…	238R1	238B4	239R1	239B4
D12	C2	0R0	0B3	1R0	1B3	…	238R0	238B3	239R0	239B3
D11	C1	0G5	0B2	1G5	1B2	…	238G5	238B2	239G5	239B2
D10	C0	0G4	0B1	1G4	1B1	…	238G4	238B1	239G4	239B1
D9		0G3	0B0	1G3	1B0	…	238G3	238B0	239G3	239B0

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

There are 2 pixels (6 sub-pixels) display data is sent by 4 transfers, when DBI [2:0] bits of 3Ah register are set to "110".

MDT[1:0]="00"

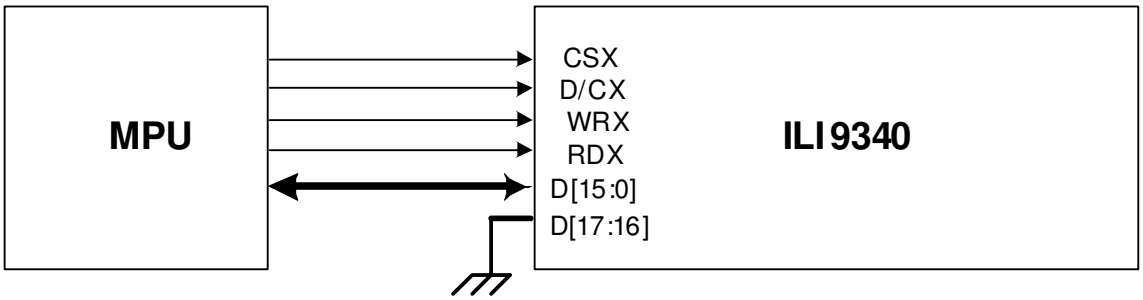
Count	0	1	2	3	4	…	478	478	479	480
D/CX	0	1	1	1	1	…	1	1	1	1
D17	C7	0R5	0G2	1R5	1G2		238R5	238G2	239R5	239G2
D16	C6	0R4	0G1	1R4	1G1	…	238R4	238G1	239R4	239G1
D15	C5	0R3	0G0	1R3	1G0	…	238R3	238G0	239R3	239G0
D14	C4	0R2	0B5	1R2	1B5	…	238R2	238B5	239R2	239B5
D13	C3	0R1	0B4	1R1	1B4	…	238R1	238B4	239R1	239B4
D12	C2	0R0	0B3	1R0	1B3	…	238R0	238B3	239R0	239B3
D11	C1	0G5	0B2	1G5	1B2	…	238G5	238B2	239G5	239B2
D10	C0	0G4	0B1	1G4	1B1	…	238G4	238B1	239G4	239B1
D9		0G3	0B0	1G3	1B0	…	238G3	238B0	239G3	239B0

MDT[1:0]="01"

Count	0	1	2	3	…	718	719	720
D/CX	0	1	1	1	…	1	1	1
D17	C7							
D16	C6	0R5	0G5	0B5	…	239R5	239G5	239B5
D15	C5	0R4	0G4	0B4	…	239R4	239G4	239B4
D14	C4	0R3	0G3	0B3	…	239R3	239G3	239B3
D13	C3	0R2	0G2	0B2	…	239R2	239G2	239B2
D12	C2	0R1	0G1	0B1	…	239R1	239G1	239B1
D11	C1	0R0	0G0	0B0	…	239R0	239G0	239B0
D10	C0				…			
D9					…			

7.6.5. 16-bit Parallel MCU Interface

The 8080-Ⅰ system 16-bit parallel bus interface of ILI9340 can be selected by setting hardware pin IM[3:0] to "0001".The following shown figure is the example of interface with 8080-Ⅰ MCU system interface.



Different display data format is available for two colors depth supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	…	238	239	240
D/CX	0	1	1	1	…	1	1	1
D15		0R4	1R4	2R4	…	237R4	238R4	239R4
D14		0R3	1R3	2R3	…	237R3	238R3	239R3
D13		0R2	1R2	2R2	…	237R2	238R2	239R2
D12		0R1	1R1	2R1	…	237R1	238R1	239R1
D11		0R0	1R0	2R0	…	237R0	238R0	239R0
D10		0G5	1G5	2G5	…	237G5	238G5	239G5
D9		0G4	1G4	2G4	…	237G4	238G4	239G4
D8		0G3	1G3	2G3	…	237G3	238G3	239G3
D7	C7	0G2	1G2	2G2	…	237G2	238G2	239G2
D6	C6	0G1	1G1	2G1	…	237G1	238G1	239G1
D5	C5	0G0	1G0	2G0	…	237G0	238G0	239G0
D4	C4	0B4	1B4	2B4	…	237B4	238B4	239B4
D3	C3	0B3	1B3	2B3	…	237B3	238B3	239B3
D2	C2	0B2	1B2	2B2	…	237B2	238B2	239B2
D1	C1	0B1	1B1	2B1	…	237B1	238B1	239B1
D0	C0	0B0	1B0	2B0	…	237B0	238B0	239B0

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 2 transfers when DBI [2:0] bits of 3Ah register are set to “110”.

MDT[1:0]=”00”

Count	0	1	2	3	…	358	359	360
D/CX	0	1	1	1	…	1	1	1
D15		0R5	0B5	1G5	…	238R5	238B5	239G5
D14		0R4	0B4	1G4	…	238R4	238B4	239G4
D13		0R3	0B3	1G3	…	238R3	238B3	239G3
D12		0R2	0B2	1G2	…	238R2	238B2	239G2
D11		0R1	0B1	1G1	…	238R1	238B1	239G1
D10		0R0	0B0	1G0	…	238R0	238B0	239G0
D9					…			
D8					…			
D7	C7	0G5	1R5	1B5	…	238G5	239R5	239B5
D6	C6	0G4	1R4	1B4	…	238G4	239R4	239B4
D5	C5	0G3	1R3	1B3	…	238G3	239R3	239B3
D4	C4	0G2	1R2	1B2	…	238G2	239R2	239B2
D3	C3	0G1	1R1	1B1	…	238G1	239R1	239B1
D2	C2	0G0	1R0	1B0	…	238G0	239R0	239B0
D1	C1				…			
D0	C0				…			

MDT[1:0]=”01”

Count	0	1	2	3		…	357	358	479	480
D/CX	0	1	1	1		…		1	1	1
D15		0R5	0B5	1R5	1B5	…	238R5	238B5	239R5	239B5
D14		0R4	0B4	1R4	1B4	…	238R4	238B4	239R4	239B4
D13		0R3	0B3	1R3	1B3	…	238R3	238B3	239R3	239B3
D12		0R2	0B2	1R2	1B2	…	238R2	238B2	239R2	239B2
D11		0R1	0B1	1R1	1B1	…	238R1	238B1	239R1	239B1
D10		0R0	0B0	1R0	1B0	…	238R0	238B0	239R0	239B0
D9						…				
D8						…				
D7	C7	0G5		1G5		…	238G5		239G5	
D6	C6	0G4		1G4		…	238G4		239G4	
D5	C5	0G3		1G3		…	238G3		239G3	
D4	C4	0G2		1G2		…	238G2		239G2	
D3	C3	0G1		1G1		…	238G1		239G1	
D2	C2	0G0		1G0		…	238G0		239G0	
D1	C1					…				
D0	C0					…				

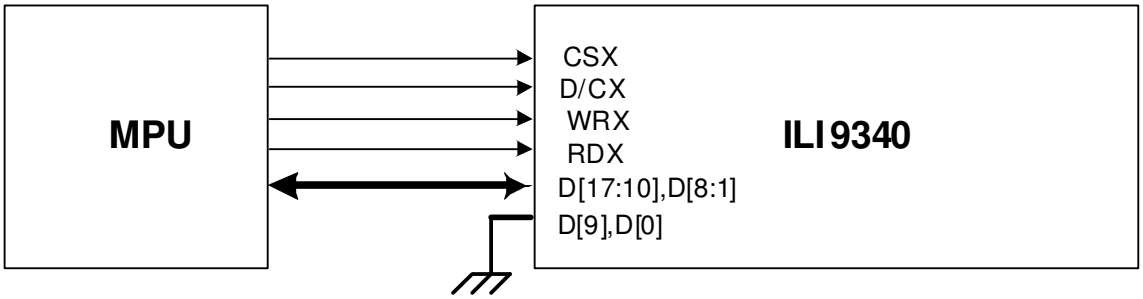
MDT[1:0]=”10”

Count	0	1	2	3		…	357	358	479	480
D/CX	0	1	1	1		…		1	1	1
D15		0R5	0B1	1R5	1B1	…	238R5	238B1	239R5	239B1
D14		0R4	0B0	1R4	1B0	…	238R4	238B0	239R4	239B0
D13		0R3		1R3		…	238R3		239R3	
D12		0R2		1R2		…	238R2		239R2	
D11		0R1		1R1		…	238R1		239R1	
D10		0R0		1R0		…	238R0		239R0	
D9		0G5		1G5		…	238G5		239G5	
D8		0G4		1G4		…	238G4		239G4	
D7	C7	0G3		1G3		…	238G3		239G3	
D6	C6	0G2		1G2		…	238G2		239G2	
D5	C5	0G1		1G1		…	238G1		239G1	
D4	C4	0G0		1G0		…	238G0		239G0	
D3	C3	0B5		1B5		…	238B5		239B5	
D2	C2	0B4		1B4		…	238B4		239B4	
D1	C1	0B3		1B3		…	238B3		239B3	
D0	C0	0B2		1B2		…	238B2		239B2	

MDT[1:0]=”11”

Count	0	1	2	3		…	357	358	479	480
D/CX	0	1	1	1		…		1	1	1
D15			0R3		1R3	…		238R3		239R3
D14			0R2		1R2	…		238R2		239R2
D13			0R1		1R1	…		238R1		239R1
D12			0R0		1R0	…		238R0		239R0
D11			0G5		1G5	…		238G5		239G5
D10			0G4		1G4	…		238G4		239G4
D9			0G3		1G3	…		238G3		239G3
D8			0G2		1G2	…		238G2		239G2
D7	C7		0G1		1G1	…		238G1		239G1
D6	C6		0G0		1G0	…		238G0		239G0
D5	C5		0B5		1B5	…		238B5		239B5
D4	C4		0B4		1B4	…		238B4		239B4
D3	C3		0B3		1B3	…		238B3		239B3
D2	C2		0B2		1B2	…		238B2		239B2
D1	C1	0R5	0B1	1R5	1B1	…	238R5	238B1	239R5	239B1
D0	C0	0R4	0B0	1R4	1B0	…	238R4	238B0	239R4	239B0

The 8080-Ⅱ system 16-bit parallel bus interface of ILI9340 can be selected by settings IM [3:0] ="1001". The following shown figure is the example of interface with 8080-Ⅱ MCU system interface.



Different display data format is available for two colors depth supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	…	238	239	240
D/CX	0	1	1	1	…	1	1	1
D17		0R4	1R4	2R4	…	237R4	238R4	239R4
D16		0R3	1R3	2R3	…	237R3	238R3	239R3
D15		0R2	1R2	2R2	…	237R2	238R2	239R2
D14		0R1	1R1	2R1	…	237R1	238R1	239R1
D13		0R0	1R0	2R0	…	237R0	238R0	239R0
D12		0G5	1G5	2G5	…	237G5	238G5	239G5
D11		0G4	1G4	2G4	…	237G4	238G4	239G4
D10		0G3	1G3	2G3	…	237G3	238G3	239G3
D8	C7	0G2	1G2	2G2	…	237G2	238G2	239G2
D7	C6	0G1	1G1	2G1	…	237G1	238G1	239G1
D6	C5	0G0	1G0	2G0	…	237G0	238G0	239G0
D5	C4	0B4	1B4	2B4	…	237B4	238B4	239B4
D4	C3	0B3	1B3	2B3	…	237B3	238B3	239B3
D3	C2	0B2	1B2	2B2	…	237B2	238B2	239B2
D2	C1	0B1	1B1	2B1	…	237B1	238B1	239B1
D1	C0	0B0	1B0	2B0	…	237B0	238B0	239B0

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 2 transfers when DBI [2:0] bits of 3Ah register are set to “110”.

MDT[1:0]=”00”

Count	0	1	2	3	…	358	359	360
D/CX	0	1	1	1	…	1	1	1
D17		0R5	0B5	1G5	…	238R5	238B5	239G5
D16		0R4	0B4	1G4	…	238R4	238B4	239G4
D15		0R3	0B3	1G3	…	238R3	238B3	239G3
D14		0R2	0B2	1G2	…	238R2	238B2	239G2
D13		0R1	0B1	1G1	…	238R1	238B1	239G1
D12		0R0	0B0	1G0	…	238R0	238B0	239G0
D11					…			
D10					…			
D8	C7	0G5	1R5	1B5	…	238G5	239R5	239B5
D7	C6	0G4	1R4	1B4	…	238G4	239R4	239B4
D6	C5	0G3	1R3	1B3	…	238G3	239R3	239B3
D5	C4	0G2	1R2	1B2	…	238G2	239R2	239B2
D4	C3	0G1	1R1	1B1	…	238G1	239R1	239B1
D3	C2	0G0	1R0	1B0	…	238G0	239R0	239B0
D2	C1				…			
D1	C0				…			

MDT[1:0]=”01”

Count	0	1	2	3		…	357	358	479	480
D/CX	0	1	1	1		…		1	1	1
D17		0R5	0B5	1R5	1B5	…	238R5	238B5	239R5	239B5
D16		0R4	0B4	1R4	1B4	…	238R4	238B4	239R4	239B4
D15		0R3	0B3	1R3	1B3	…	238R3	238B3	239R3	239B3
D14		0R2	0B2	1R2	1B2	…	238R2	238B2	239R2	239B2
D13		0R1	0B1	1R1	1B1	…	238R1	238B1	239R1	239B1
D12		0R0	0B0	1R0	1B0	…	238R0	238B0	239R0	239B0
D11						…				
D10						…				
D8	C7	0G5		1G5		…	238G5		239G5	
D7	C6	0G4		1G4		…	238G4		239G4	
D6	C5	0G3		1G3		…	238G3		239G3	
D5	C4	0G2		1G2		…	238G2		239G2	
D4	C3	0G1		1G1		…	238G1		239G1	
D3	C2	0G0		1G0		…	238G0		239G0	
D2	C1					…				
D1	C0					…				

MDT[1:0]=”10”

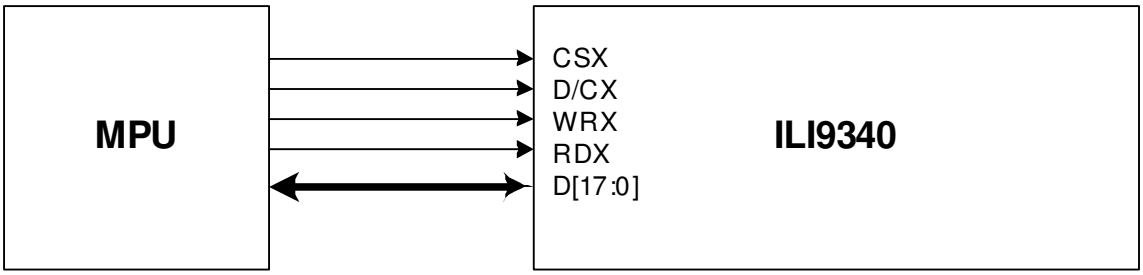
Count	0	1	2	3		…	357	358	479	480
D/CX	0	1	1	1		…		1	1	1
D17		0R5	0B1	1R5	1B1	…	238R5	238B1	239R5	239B1
D16		0R4	0B0	1R4	1B0	…	238R4	238B0	239R4	239B0
D15		0R3		1R3		…	238R3		239R3	
D14		0R2		1R2		…	238R2		239R2	
D13		0R1		1R1		…	238R1		239R1	
D12		0R0		1R0		…	238R0		239R0	
D11		0G5		1G5		…	238G5		239G5	
D10		0G4		1G4		…	238G4		239G4	
D8	C7	0G3		1G3		…	238G3		239G3	
D7	C6	0G2		1G2		…	238G2		239G2	
D6	C5	0G1		1G1		…	238G1		239G1	
D5	C4	0G0		1G0		…	238G0		239G0	
D4	C3	0B5		1B5		…	238B5		239B5	
D3	C2	0B4		1B4		…	238B4		239B4	
D2	C1	0B3		1B3		…	238B3		239B3	
D1	C0	0B2		1B2		…	238B2		239B2	

MDT[1:0]=”11”

Count	0	1	2	3		…	357	358	479	480
D/CX	0	1	1	1		…		1	1	1
D17			0R3		1R3	…		238R3		239R3
D16			0R2		1R2	…		238R2		239R2
D15			0R1		1R1	…		238R1		239R1
D14			0R0		1R0	…		238R0		239R0
D13			0G5		1G5	…		238G5		239G5
D12			0G4		1G4	…		238G4		239G4
D11			0G3		1G3	…		238G3		239G3
D10			0G2		1G2	…		238G2		239G2
D8	C7		0G1		1G1	…		238G1		239G1
D7	C6		0G0		1G0	…		238G0		239G0
D6	C5		0B5		1B5	…		238B5		239B5
D5	C4		0B4		1B4	…		238B4		239B4
D4	C3		0B3		1B3	…		238B3		239B3
D3	C2		0B2		1B2	…		238B2		239B2
D2	C1	0R5	0B1	1R5	1B1	…	238R5	238B1	239R5	239B1
D1	C0	0R4	0B0	1R4	1B0	…	238R4	238B0	239R4	239B0

7.6.6. 18-bit Parallel MCU Interface

The 8080-Ⅰ system 18-bit parallel bus interface of ILI9340 can be selected by setting hardware pin IM[3:0] to "0011".The following shown figure is the example of interface with 8080-Ⅰ MCU system interface.



Different display data format is available for one color depth only supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "101".

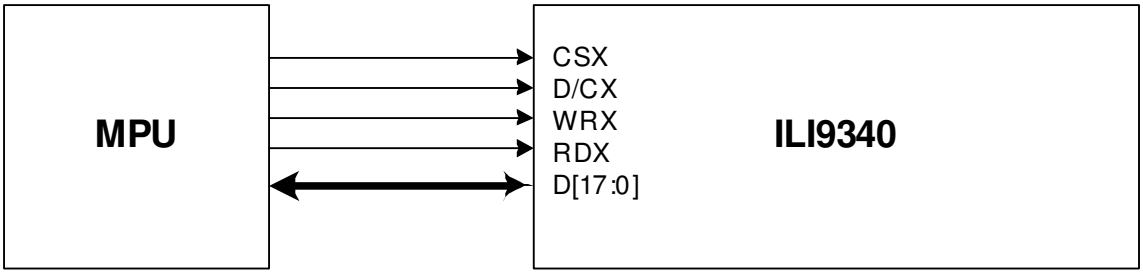
Count	0	1	2	3	…	238	239	240
D/CX	0	1	1	1	…	1	1	1
D17								
D16								
D15		0R4	1R4	2R4	…	237R4	238R4	239R4
D14		0R3	1R3	2R3	…	237R3	238R3	239R3
D13		0R2	1R2	2R2	…	237R2	238R2	239R2
D12		0R1	1R1	2R1	…	237R1	238R1	239R1
D11		0R0	1R0	2R0	…	237R0	238R0	239R0
D10		0G5	1G5	2G5	…	237G5	238G5	239G5
D9		0G4	1G4	2G4	…	237G4	238G4	239G4
D8		0G3	1G3	2G3	…	237G3	238G3	239G3
D7	C7	0G2	1G2	2G2	…	237G2	238G2	239G2
D6	C6	0G1	1G1	2G1	…	237G1	238G1	239G1
D5	C5	0G0	1G0	2G0	…	237G0	238G0	239G0
D4	C4	0B4	1B4	2B4	…	237B4	238B4	239B4
D3	C3	0B3	1B3	2B3	…	237B3	238B3	239B3
D2	C2	0B2	1B2	2B2	…	237B2	238B2	239B2
D1	C1	0B1	1B1	2B1	…	237B1	238B1	239B1
D0	C0	0B0	1B0	2B0	…	237B0	238B0	239B0

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to “110”.

Count	0	1	2	3	…	238	239	240
D/CX	0	1	1	1	…	1	1	1
D17		0R5	1R5	2R5	…	237R5	238R5	239R5
D16		0R4	1R4	2R4	…	237R4	238R4	239R4
D15		0R3	1R3	2R3	…	237R3	238R3	239R3
D14		0R2	1R2	2R2	…	237R2	238R2	239R2
D13		0R1	1R1	2R1	…	237R1	238R1	239R1
D12		0R0	1R0	2R0	…	237R0	238R0	239R0
D11		0G5	1G5	2G5	…	237G5	238G5	239G5
D10		0G4	1G4	2G4	…	237G4	238G4	239G4
D9		0G3	1G3	2G3	…	237G3	238G3	239G3
D8		0G2	1G2	2G2	…	237G2	238G2	239G2
D7	C7	0G1	1G1	2G1	…	237G1	238G1	239G1
D6	C6	0G0	1G0	2G0	…	237G0	238G0	239G0
D5	C5	0B5	1B5	2B5	…	237B5	238B5	239B5
D4	C4	0B4	1B4	2B4	…	237B4	238B4	239B4
D3	C3	0B3	1B3	2B3	…	237B3	238B3	239B3
D2	C2	0B2	1B2	2B2	…	237B2	238B2	239B2
D1	C1	0B1	1B1	2B1	…	237B1	238B1	239B1
D0	C0	0B0	1B0	2B0	…	237B0	238B0	239B0

The 8080-Ⅱ system 18-bit parallel bus interface mode can be selected by settings IM [3:0] ="1011". The following shown figure is the example of interface with 8080-Ⅱ MCU system interface.



Different display data format is available for one color depth only supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	…	238	239	240
D/CX	0	1	1	1	…	1	1	1
D17								
D16								
D15		0R4	1R4	2R4	…	237R4	238R4	239R4
D14		0R3	1R3	2R3	…	237R3	238R3	239R3
D13		0R2	1R2	2R2	…	237R2	238R2	239R2
D12		0R1	1R1	2R1	…	237R1	238R1	239R1
D11		0R0	1R0	2R0	…	237R0	238R0	239R0
D10		0G5	1G5	2G5	…	237G5	238G5	239G5
D9		0G4	1G4	2G4	…	237G4	238G4	239G4
D8	C7	0G3	1G3	2G3	…	237G3	238G3	239G3
D7	C6	0G2	1G2	2G2	…	237G2	238G2	239G2
D6	C5	0G1	1G1	2G1	…	237G1	238G1	239G1
D5	C4	0G0	1G0	2G0	…	237G0	238G0	239G0
D4	C3	0B4	1B4	2B4	…	237B4	238B4	239B4
D3	C2	0B3	1B3	2B3	…	237B3	238B3	239B3
D2	C1	0B2	1B2	2B2	…	237B2	238B2	239B2
D1	C0	0B1	1B1	2B1	…	237B1	238B1	239B1
D0		0B0	1B0	2B0	…	237B0	238B0	239B0

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

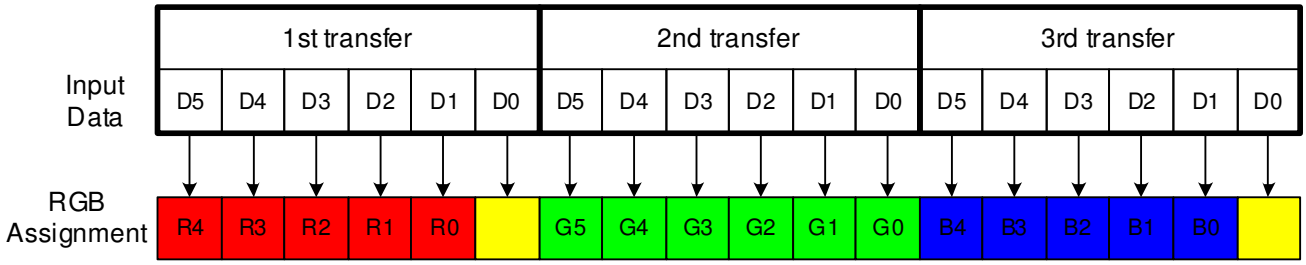
One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to “110”.

Count	0	1	2	3	…	238	239	240
D/CX	0	1	1	1	…	1	1	1
D17		0R5	1R5	2R5	…	237R5	238R5	239R5
D16		0R4	1R4	2R4	…	237R4	238R4	239R4
D15		0R3	1R3	2R3	…	237R3	238R3	239R3
D14		0R2	1R2	2R2	…	237R2	238R2	239R2
D13		0R1	1R1	2R1	…	237R1	238R1	239R1
D12		0R0	1R0	2R0	…	237R0	238R0	239R0
D11		0G5	1G5	2G5	…	237G5	238G5	239G5
D10		0G4	1G4	2G4	…	237G4	238G4	239G4
D9		0G3	1G3	2G3	…	237G3	238G3	239G3
D8	C7	0G2	1G2	2G2	…	237G2	238G2	239G2
D7	C6	0G1	1G1	2G1	…	237G1	238G1	239G1
D6	C5	0G0	1G0	2G0	…	237G0	238G0	239G0
D5	C4	0B5	1B5	2B5	…	237B5	238B5	239B5
D4	C3	0B4	1B4	2B4	…	237B4	238B4	239B4
D3	C2	0B3	1B3	2B3	…	237B3	238B3	239B3
D2	C1	0B2	1B2	2B2	…	237B2	238B2	239B2
D1	C0	0B1	1B1	2B1	…	237B1	238B1	239B1
D0		0B0	1B0	2B0	…	237B0	238B0	239B0

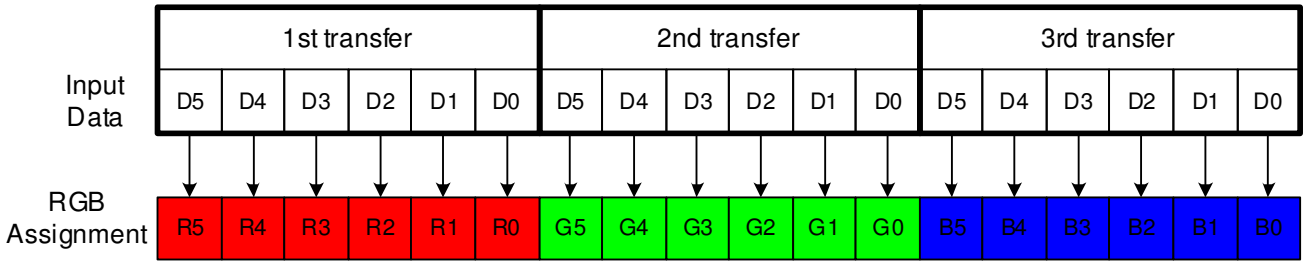
7.6.7. 6-bit Parallel RGB Interface

The 6-bit RGB interface is selected by setting the DPI [2:0] bit to “110”. When RCM [1:0] are set to “10” and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data are transferred to the internal GRAM in synchronization with the display operation via 6-bit RGB data bus (D [5:0]) according to the data enable signal (DE) when RCM [1:0] are set to “10”. The RGB interface SYNC mode is selected by setting the RCM [1:0] to “11”, the valid display data is inputted in pixel unit via D [5:0] according to the VFP/VBP and HFP/HBP settings. Unused pins must be connected to GND to ensure normally operation. Registers can be set by the SPI system interface.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)



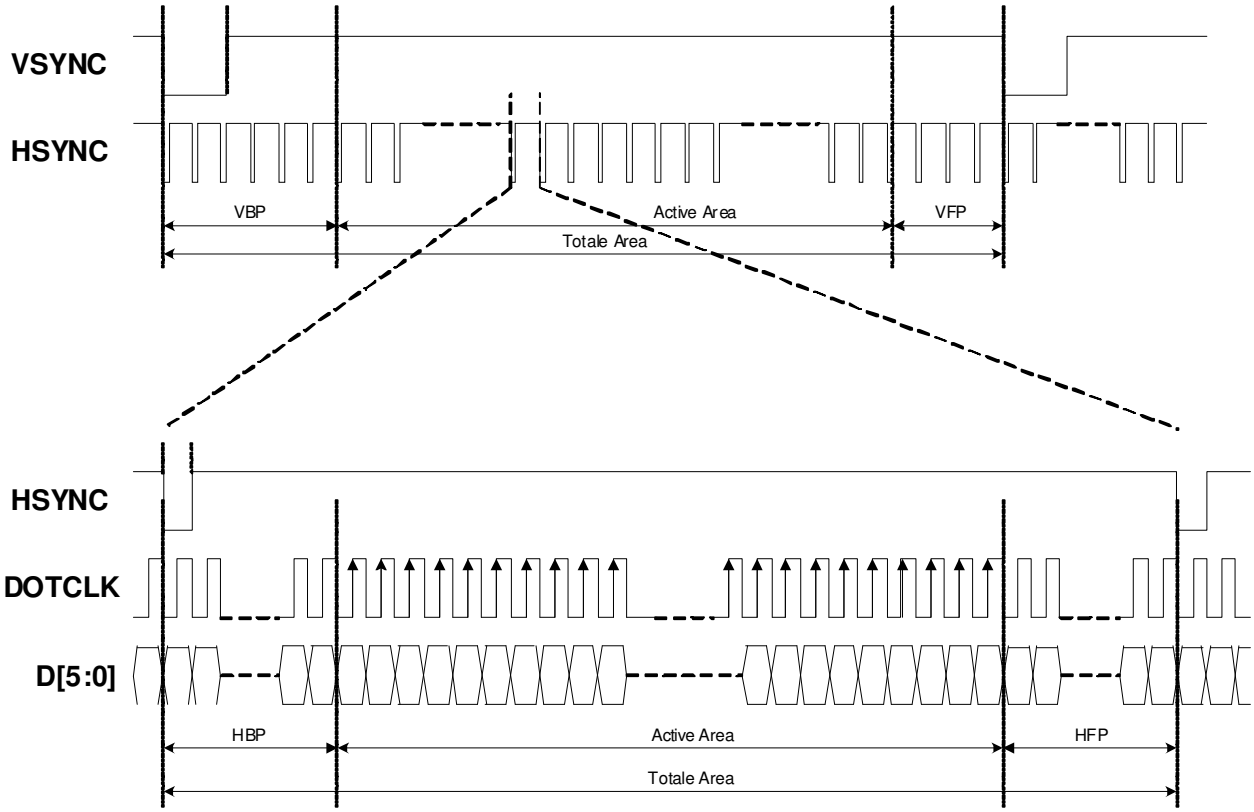
262K color: 18-bit/pixel (RGB 6-6-6 bits input)



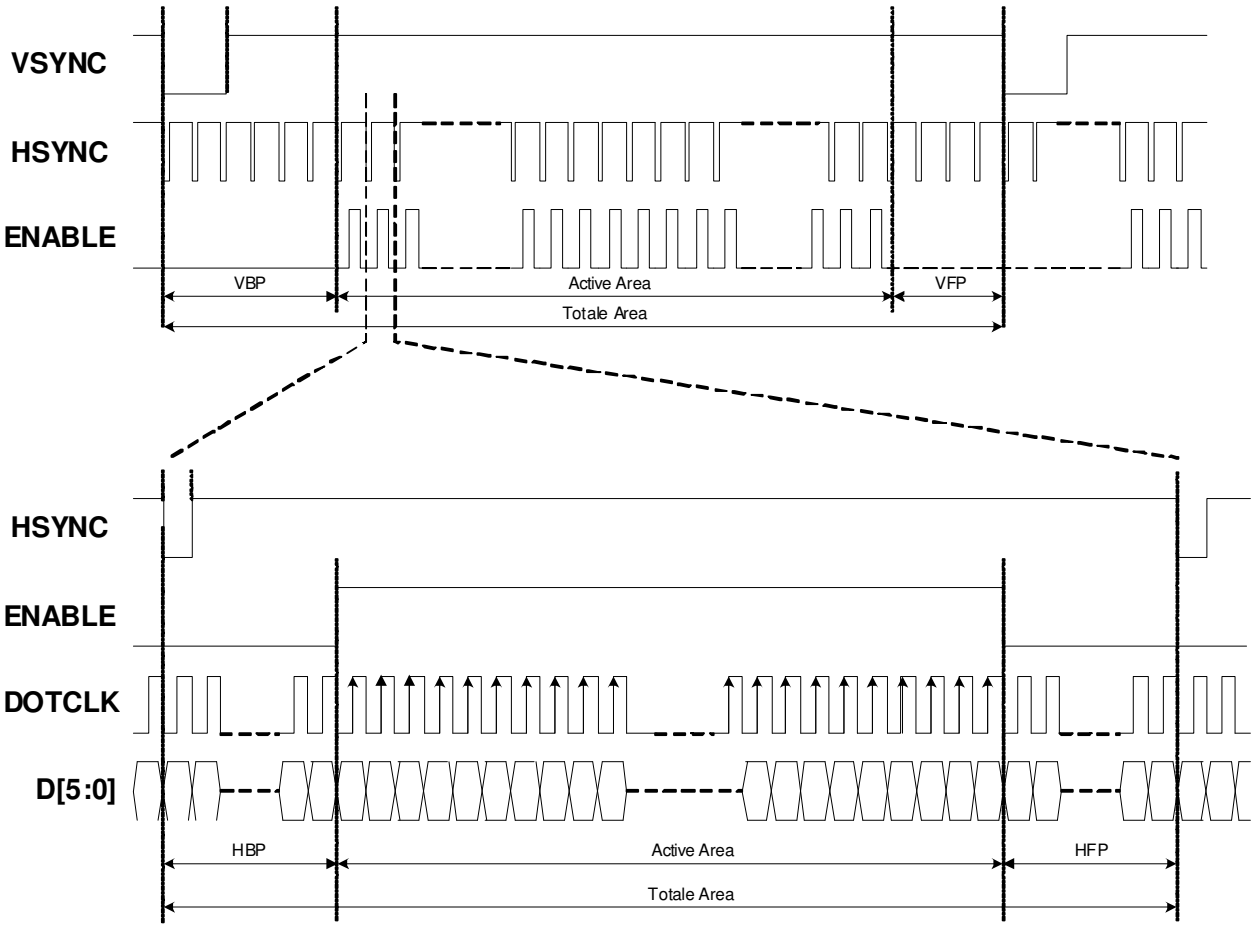
ILI9340 has data transfer counters to count the first, second, third data transfer in 6-bit RGB interface mode. The transfer counter is always reset to the state of first data transfer on the falling edge of VSYNC. If a mismatch arises in the number of each data transfer, the counter is reset to the state of first data transfer at the start of the frame (i.e. on the falling edge of VSYNC) to restart data transfer in the correct order from the next frame. This function is expedient for moving picture display, which requires consecutive data transfer in light of minimizing effects from failed data transfer and enabling the system to return to a normal state.

Note that internal display operation is performed in units of pixels (RGB: taking 3 inputs of DOTCLK). Accordingly, the number of DOTCLK inputs in one frame period must be a multiple of 3 to complete data transfer correctly. Otherwise it will affect the display of that frame as well as the next frame.

SYNC Mode, RCM[1:0]="11"

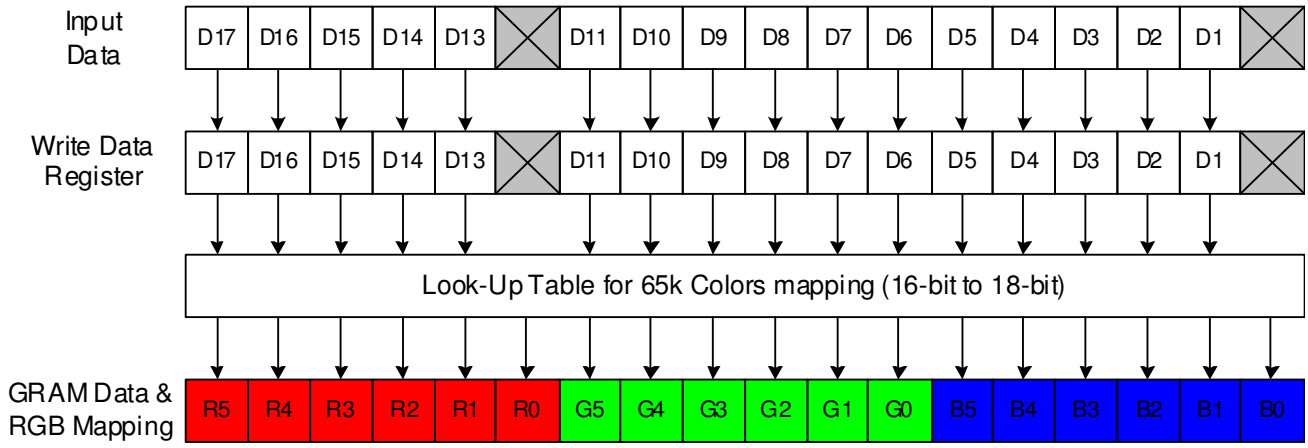


DE Mode, RCM[1:0]="10"



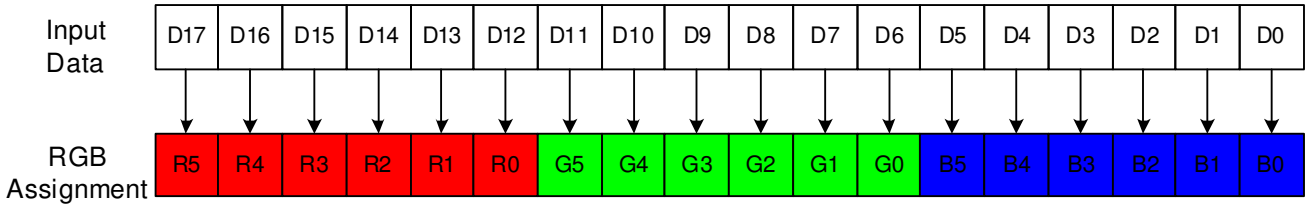
7.6.8. 16-bit Parallel RGB Interface

The 16-bit RGB interface is selected by setting the DPI [2:0] bits to “101”. When RCM [1:0] are set to “10” and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data is transferred to the internal GRAM in synchronization with the display operation via 16-bit RGB data bus (D [17:13] & D [11:1]) according to the data enable signal (DE). The RGB interface SYNC mode is selected by setting the RCM [1:0] to “11”, the valid display data is inputted in pixel unit via D [17:13] and D [11:1] according to the VFP/VBP and HFP/HBP settings. The unused D12 and D0 pins must be connected to GND for ensure normally operation. Registers can be set by the SPI system interface.



7.6.9. 18-bit Parallel RGB Interface

The 18-bit RGB interface is selected by setting the DPI [2:0] bits to “110”. When RCM [1:0] are set to “10” and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data are transferred to the internal GRAM in synchronization with the display operation via 18-bit RGB data bus (D [17:0]) according to the data enable signal (DE) when RCM [1:0] are set to “10”. The RGB interface SYNC mode is selected by setting the RCM [1:0] to “11”, the valid display data is inputted in pixel unit via D [17:0] according to the VFP/VBP and HFP/HBP settings. Registers can be set by the SPI system interface.



8. Command

8.1. Command List

Regulative Command Set													
Command Function	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex
No Operation	0	1	↑	XX	0	0	0	0	0	0	0	0	00h
Software Reset	0	1	↑	XX	0	0	0	0	0	0	0	1	01h
Read Display Identification Information	0	1	↑	XX	0	0	0	0	0	1	0	0	04h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	ID1 [7:0]								XX
	1	↑	1	XX	ID2 [7:0]								XX
	1	↑	1	XX	ID3 [7:0]								XX
Read Display Status	0	1	↑	XX	0	0	0	0	1	0	0	1	09h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D [31:25]							X	00
	1	↑	1	XX	X	D [22:20]			D [19:16]				61
	1	↑	1	XX	X	X	X	X	X	D [10:8]			00
	1	↑	1	XX	D [7:5]			X	X	X	X	X	00
Read Display Power Mode	0	1	↑	XX	0	0	0	0	1	0	1	0	0Ah
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D [7:2]						0	0	08
Read Display MADCTL	0	1	↑	XX	0	0	0	0	1	0	1	1	0Bh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D [7:2]						0	0	00
Read Display Pixel Format	0	1	↑	XX	0	0	0	0	1	1	0	0	0Ch
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	RIM	DPI [2:0]			X	DBI [2:0]			06
Read Display Image Format	0	1	↑	XX	0	0	0	0	1	1	0	1	0Dh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	X	X	X	X	X	D [2:0]			00
Read Display Signal Mode	0	1	↑	XX	0	0	0	0	1	1	1	0	0Eh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D [7:2]						0	0	00
Read Display Self-Diagnostic Result	0	1	↑	XX	0	0	0	0	1	1	1	1	0Fh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D [7:6]		X	X	X	X	X	X	00
Enter Sleep Mode	0	1	↑	XX	0	0	0	1	0	0	0	0	10h
Sleep OUT	0	1	↑	XX	0	0	0	1	0	0	0	1	11h
Partial Mode ON	0	1	↑	XX	0	0	0	1	0	0	1	0	12h
Normal Display Mode ON	0	1	↑	XX	0	0	0	1	0	0	1	1	13h
Display Inversion OFF	0	1	↑	XX	0	0	1	0	0	0	0	0	20h
Display Inversion ON	0	1	↑	XX	0	0	1	0	0	0	0	1	21h
Gamma Set	0	1	↑	XX	0	0	1	0	0	1	1	0	26h
	1	1	↑	XX	GC [7:0]								01
Display OFF	0	1	↑	XX	0	0	1	0	1	0	0	0	28h
Display ON	0	1	↑	XX	0	0	1	0	1	0	0	1	29h
Column Address Set	0	1	↑	XX	0	0	1	0	1	0	1	0	2Ah
	1	1	↑	XX	SC [15:8]								XX
	1	1	↑	XX	SC [7:0]								XX
	1	1	↑	XX	EC [15:8]								XX
	1	1	↑	XX	EC [7:0]								XX
Page Address Set	0	1	↑	XX	0	0	1	0	1	0	1	1	2Bh
	1	1	↑	XX	SP [15:8]								XX
	1	1	↑	XX	SP [7:0]								XX
	1	1	↑	XX	EP [15:8]								XX
	1	1	↑	XX	EP [7:0]								XX

Memory Write	0	1	↑	XX	0	0	1	0	1	1	0	0	2Ch
	1	1	↑	D [17:0]									XX
Color SET	0	1	↑	XX	0	0	1	0	1	1	0	1	2Dh
	1	↑	1	XX	R00 [5:0]								XX
	1	↑	1	XX	Rnn [5:0]								XX
	1	↑	1	XX	R31 [5:0]								XX
	1	↑	1	XX	G00 [5:0]								XX
	1	↑	1	XX	Gnn [5:0]								XX
	1	↑	1	XX	G63 [5:0]								XX
	1	↑	1	XX	B00 [5:0]								XX
	1	↑	1	XX	Bnn [5:0]								XX
	1	↑	1	XX	B31 [5:0]								XX
Memory Read	0	1	↑	XX	0	0	1	0	1	1	1	0	2Eh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	D [17:0]									XX
Partial Area	0	1	↑	XX	0	0	1	1	0	0	0	0	30h
	1	1	↑	XX	SR [15:8]								00
	1	1	↑	XX	SR [7:0]								00
	1	1	↑	XX	ER [15:8]								01
	1	1	↑	XX	ER [7:0]								3F
Vertical Scrolling Definition	0	1	↑	XX	0	0	1	1	0	0	1	1	33h
	1	1	↑	XX	TFA [15:8]								00
	1	1	↑	XX	TFA [7:0]								00
	1	1	↑	XX	VSA [15:8]								01
	1	1	↑	XX	VSA [7:0]								40
	1	1	↑	XX	BFA [15:8]								00
	1	1	↑	XX	BFA [7:0]								00
Tearing Effect Line OFF	0	1	↑	XX	0	0	1	1	0	1	0	0	34h
Tearing Effect Line ON	0	1	↑	XX	0	0	1	1	0	1	0	1	35h
	1	1	↑	XX	X	X	X	X	X	X	X	M	00
Memory Access Control	0	1	↑	XX	0	0	1	1	0	1	1	0	36h
	1	1	↑	XX	MY	MX	MV	ML	BGR	MH	X	X	00
Vertical Scrolling Start Address	0	1	↑	XX	0	0	1	1	0	1	1	1	37h
	1	1	↑	XX	VSP [15:8]								00
	1	1	↑	XX	VSP [7:0]								00
Idle Mode OFF	0	1	↑	XX	0	0	1	1	1	0	0	0	38h
Idle Mode ON	0	1	↑	XX	0	0	1	1	1	0	0	1	39h
Pixel Format Set	0	1	↑	XX	0	0	1	1	1	0	1	0	3Ah
	1	1	↑	XX	X	DPI [2:0]			X	DBI [2:0]			66
Write Memory Continue	0	1	↑	XX	0	0	1	1	1	1	0	0	3Ch
	1	1	↑	D [17:0]									XX
Read Memory Continue	0	1	↑	XX	0	0	1	1	1	1	1	0	3Eh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	D [17:0]									XX
Set Tear Scanline	0	1	↑	XX	0	1	0	0	0	1	0	0	44h
	1	1	↑	XX	X	X	X	X	X	X	X	STS [8]	00
	1	1	↑	XX	STS [7:0]								00
Get Scanline	0	1	↑	XX	0	1	0	0	0	1	0	1	45h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	X	X	X	X	X	X	GTS [9:8]		00
	1	↑	1	XX	GTS [7:0]								00
Write Display Brightness	0	1	↑	XX	0	1	0	1	0	0	0	1	51h
	1	1	↑	XX	DBV [7:0]								00

Read Display Brightness	0	1	↑	XX	0	1	0	1	0	0	1	0	52h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	DBV [7:0]								00
Write CTRL Display	0	1	↑	XX	0	1	0	1	0	0	1	1	53h
	1	1	↑	XX	X	X	BCTRL	X	DD	BL	X	X	00
Read CTRL Display	0	1	↑	XX	0	1	0	1	0	1	0	0	54h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	X	X	BCTRL	X	DD	BL	X	X	00
Write Content Adaptive Brightness Control	0	1	↑	XX	0	1	0	1	0	1	0	1	55h
	1	1	↑	XX	X	X	X	X	X	X	C [1:0]		00
Read Content Adaptive Brightness Control	0	1	↑	XX	0	1	0	1	0	1	1	0	56h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	X	X	X	X	X	X	C [1:0]		00
Write CABC Minimum Brightness	0	1	↑	XX	0	1	0	1	1	1	1	0	5Eh
	1	1	↑	XX	CMB [7:0]								00
Read CABC Minimum Brightness	0	1	↑	XX	0	1	0	1	0	1	1	1	5Fh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	CMB [7:0]								00
Read ID1	0	1	↑	XX	1	1	0	1	1	0	1	0	DAh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	Module's Manufacture [7:0]								XX
Read ID2	0	1	↑	XX	1	1	0	1	1	0	1	1	DBh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	LCD Module / Driver Version [7:0]								XX
Read ID3	0	1	↑	XX	1	1	0	1	1	1	0	0	DCh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	LCD Module / Driver ID [7:0]								XX

Extended Command Set													
Command Function	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RGB Interface Signal Control	0	1	↑	XX	1	0	1	1	0	0	0	0	B0h
	1	1	↑	XX	ByPass_MODE	RCM [1:0]		X	VSPL	HSPL	DPL	EPL	40
Frame Control (In Normal Mode)	0	1	↑	XX	1	0	1	1	0	0	0	1	B1h
	1	1	↑	XX	X	X	X	X	X	X	DIVA [1:0]		00
	1	1	↑	XX	X	X	X	RTNA [4:0]					1B
Frame Control (In Idle Mode)	0	1	↑	XX	1	0	1	1	0	0	1	0	B2h
	1	1	↑	XX	X	X	X	X	X	X	DIVB [1:0]		00
	1	1	↑	XX	X	X	X	RTNB [4:0]					1B
Frame Control (In Partial Mode)	0	1	↑	XX	1	0	1	1	0	0	1	1	B3h
	1	1	↑	XX	X	X	X	X	X	X	DIVC [1:0]		00
	1	1	↑	XX	X	X	X	RTNC [4:0]					1B
Display Inversion Control	0	1	↑	XX	1	0	1	1	0	1	0	0	B4h
	1	1	↑	XX	X	X	X	X	X	NLA	NLB	NLC	02
	1	1	↑	XX	X	X	NW [5:0]						00
Blanking Porch Control	0	1	↑	XX	1	0	1	1	0	1	0	1	B5h
	1	1	↑	XX	0	VFP [6:0]							02
	1	1	↑	XX	0	VBP [6:0]							02
	1	1	↑	XX	0	0	0	HFP [4:0]					0A
	1	1	↑	XX	0	0	0	HBP [4:0]					14

Display Function Control	0	1	↑	XX	1	0	1	1	0	1	1	0	B6h
	1	1	↑	XX	X	X	X	X	PTG [1:0]		PT [1:0]		0A
	1	1	↑	XX	REV	GS	SS	SM	ISC [3:0]				82
	1	1	↑	XX	X	X	NL [5:0]						27
	1	1	↑	XX	X	X	PCDIV [5:0]						XX
Entry Mode Set	0	1	↑	XX	1	0	1	1	0	1	1	1	B7h
	1	1	↑	XX	X	X	X	X	X	GON	DTE	GAS	07
Backlight Control 1	0	1	↑	XX	1	0	1	1	1	0	0	0	B8h
	1	1	↑	XX	X	X	X	X	X	X	X	X	XX
	1	1	↑	XX	X	X	X	X	TH_UI [3:0]				04
Backlight Control 2	0	1	↑	XX	1	0	1	1	1	0	0	1	B9h
	1	1	↑	XX	X	X	X	X	X	X	X	X	XX
	1	1	↑	XX	TH_MV [3:0]				TH_ST [3:0]				B8
Backlight Control 3	0	1	↑	XX	1	0	1	1	1	0	1	0	BAh
	1	1	↑	XX	X	X	X	X	X	X	X	X	XX
	1	1	↑	XX	X	X	X	X	DTH_UI [3:0]				04
Backlight Control 4	0	1	↑	XX	1	0	1	1	1	0	1	1	BBh
	1	1	↑	XX	X	X	X	X	X	X	X	X	XX
	1	1	↑	XX	DTH_MV [3:0]				DTH_ST [3:0]				C9
Backlight Control 5	0	1	↑	XX	1	0	1	1	1	1	0	0	BCh
	1	1	↑	XX	X	X	X	X	X	X	X	X	XX
	1	1	↑	XX	DIM2 [3:0]				X	DIM1 [2:0]			44
Backlight Control 7	0	1	↑	XX	1	0	1	1	1	1	1	0	BEh
	1	1	↑	XX	PWM_DIV [7:0]								0F
Backlight Control 8	0	1	↑	XX	1	0	1	1	1	1	1	1	BFh
	1	1	↑	XX	X	X	X	X	X	LEDONR	LEDONPOL	LEDPWMOPL	00
Power Control 1	0	1	↑	XX	1	1	0	0	0	0	0	0	C0h
	1	1	↑	XX	X	X	VRH [5:0]						26
	1	1	↑	XX	X	X	X	X	VC [3:0]				00
Power Control 2	0	1	↑	XX	1	1	0	0	0	0	0	1	C1h
	1	1	↑	XX	X	X	X	X	BT [3:0]				00
Power Control 3 (For Normal Mode)	0	1	↑	XX	1	1	0	0	0	0	1	0	C2h
	1	1	↑	XX	1	DCA1 [2:0]			0	DCA0 [2:0]			B2
Power Control 4 (For Idle Mode)	0	1	↑	XX	1	1	0	0	0	0	1	1	C3h
	1	1	↑	XX	1	DCB1 [2:0]			0	DCB0 [2:0]			B2
Power Control 5 (For Partial Mode)	0	1	↑	XX	1	1	0	0	0	1	0	0	C4h
	1	1	↑	XX	1	DCC1 [2:0]			0	DCC0 [2:0]			B2
VCOM Control 1	0	1	↑	XX	1	1	0	0	0	1	0	1	C5h
	1	1	↑	XX	X	VMH [6:0]							31
	1	1	↑	XX	X	VML [6:0]							3C
VCOM Control 2	0	1	↑	XX	1	1	0	0	0	1	1	1	C7h
	1	1	↑	XX	nVM	VMF [6:0]							C0
NV Memory Write	0	1	↑	XX	1	1	0	1	0	0	0	0	D0h
	1	1	↑	XX	X	X	X	X	X	PGM_ADR [2:0]			00
	1	1	↑	XX	PGM_DATA [7:0]								XX
NV Memory Protection Key	0	1	↑	XX	1	1	0	1	0	0	0	1	D1h
	1	1	↑	XX	KEY [23:16]								55
	1	1	↑	XX	KEY [15:8]								AA
	1	1	↑	XX	KEY [7:0]								66
NV Memory Status Read	0	1	↑	XX	1	1	0	1	0	0	1	0	D2h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	X	ID2_CNT [2:0]			X	ID1_CNT [2:0]			XX
	1	↑	1	XX	BUSY	VMF_CNT [2:0]			X	ID3_CNT [2:0]			XX

Read ID4	0	↑	1	XX	1	1	0	1	0	0	1	1	D3h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	0	1	0	0	0	0	0	0	40
Positive Gamma Correction	0	1	↑	XX	1	1	1	0	0	0	0	0	E0h
	1	1	↑	XX	X	X	X	X	VP0 [3:0]				0F
	1	1	↑	XX	X	X	VP1 [5:0]						22
	1	1	↑	XX	X	X	VP2 [5:0]						1F
	1	1	↑	XX	X	X	X	X	VP4 [3:0]				0A
	1	1	↑	XX	X	X	X	VP6 [4:0]					0E
	1	1	↑	XX	X	X	X	X	VP13 [3:0]				06
	1	1	↑	XX	X	VP20 [6:0]							4D
	1	1	↑	XX	VP36 [3:0]				VP27 [3:0]				76
	1	1	↑	XX	X	VP43 [6:0]							3B
	1	1	↑	XX	X	X	X	X	VP50 [3:0]				03
	1	1	↑	XX	X	X	X	VP57 [4:0]					0E
	1	1	↑	XX	X	X	X	X	VP59 [3:0]				04
	1	1	↑	XX	X	X	VP61 [5:0]						13
	1	1	↑	XX	X	X	VP62 [5:0]						0E
	1	1	↑	XX	X	X	X	X	VP63 [3:0]				0C
Negative Gamma CorrectionE	0	1	↑	XX	1	1	1	0	0	0	0	1	E1h
	1	1	↑	XX	X	X	X	X	VN0 [4:0]				0C
	1	1	↑	XX	X	X	VN1 [5:0]						23
	1	1	↑	XX	X	X	VN2 [5:0]						26
	1	1	↑	XX	X	X	X	X	VN4 [3:0]				04
	1	1	↑	XX	X	X	X	VN6 [4:0]					10
	1	1	↑	XX	X	X	X	X	VN13 [3:0]				04
	1	1	↑	XX	X	VN20 [6:0]							39
	1	1	↑	XX	VN36 [3:0]				VN27 [3:0]				24
	1	1	↑	XX	X	VN43 [6:0]							4B
	1	1	↑	XX	X	X	X	X	VN50 [3:0]				03
	1	1	↑	XX	X	X	X	VN57 [4:0]					0B
	1	1	↑	XX	X	X	X	X	VN59 [3:0]				0B
	1	1	↑	XX	X	X	VN61 [5:0]						33
	1	1	↑	XX	X	X	VN62 [5:0]						37
	1	1	↑	XX	X	X	X	X	VN63 [4:0				0F
Digital Gamma Control 1	0	1	↑	XX	1	1	1	0	0	0	1	0	E2h
1st Parameter	1	1	↑	XX	RCA0 [3:0]				BCA0 [3:0]				XX
:	1	1	↑	XX	RCAx [3:0]				BCAx [3:0]				XX
16th Parameter	1	1	↑	XX	RCA15 [3:0]				BCA15 [3:0]				XX
Digital Gamma Control 2	0	1	↑	XX	1	1	1	0	0	0	1	1	E3h
1st Parameter	1	1	↑	XX	RFA0 [3:0]				BFA0 [3:0]				XX
:	1	1	↑	XX	RFAx [3:0]				BFAx [3:0]				XX
64th Parameter	1	1	↑	XX	RFA63 [3:0]				BFA63 [3:0]				XX
3 Gamma control	0	1	↑	XX	1	1	1	1	0	0	1	0	F2h
	1	1	↑	XX	X	X	X	X	X	X	En_dith	En_3g	10
Interface Control	0	1	↑	XX	1	1	1	1	0	1	1	0	F6h
	1	1	↑	XX	MY_EOR	MX_EOR	MV_EOR	X	BGR_EOR	X	X	WEMODE	01
	1	1	↑	XX	X	X	EPF [1:0]		X	X	MDT [1:0]		00
	1	1	↑	XX	X	X	ENDIAN	X	DM [1:0]		RM	RIM	00

Note 1: Undefined commands are treated as NOP (00h) command.

Note 2: B0 to D9 and DE to FF are for factory use of display supplier. USER can decide if these commands are available or they are treated as NOP (00h) commands before shipping to USER. Default value is NOP (00h).

Note 3: Commands 10h, 12h, 13h, 26h, 28h, 29h, 30h, 36h (Bit B4 only), 38h and 39h are updated during V-SYNC when ILI9340 is in Sleep OUT mode to avoid abnormal visual effects. During Sleep IN mode, these commands are updated immediately. Read status (09h), Read display power mode (0Ah), Read display MADCTL (0Bh), Read display pixel format (0Ch), Read display image mode (0Dh), Read display signal mode (0Eh) and Read display self diagnostic result (0Fh) of these commands are updated immediately both in Sleep IN mode and Sleep OUT mode.

8.2. Description of Level 1 Command

8.2.1. NOP (00h)

<table>
<tr><th>00h</th><th colspan="13">NOP (No Operation)</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter.</td></tr>
<tr><td>Description</td><td colspan="13">This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read as described in RAMWR (Memory Write) and RAMRD (Memory Read) Commands.
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">None</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>SW Reset</td><td>N/A</td></tr><tr><td>HW Reset</td><td>N/A</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">None</td></tr>
</table>

8.2.2. Software Reset (01h)

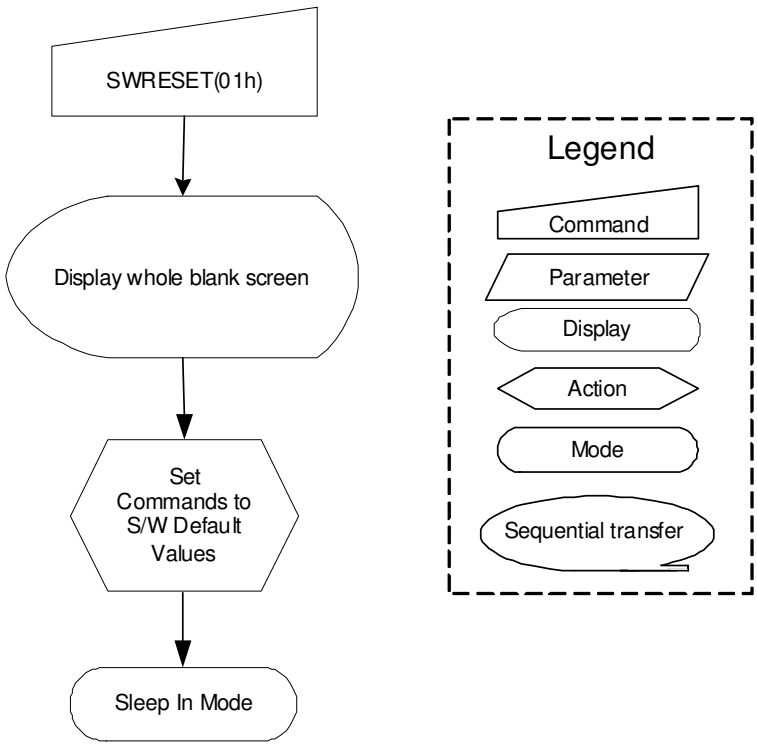
01h	SWRESET												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	0	0	0	1	01h
Parameter	No Parameter.												
Description	When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.) Note: The Frame Memory contents are unaffected by this command X = Don't care.												
Restriction	It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display supplier factory default values to the registers during this 5msec. If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep out command. Software Reset Command cannot be sent during Sleep Out sequence.												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
SW Reset	N/A
HW Reset	N/A

Flow Chart



8.2.3. Read display identification information (04h)

04h	RDDIDIF (Read Display Identification Information)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	0	1	0	0	04h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2ndParameter	1	↑	1	XX	ID1 [7:0]								XX
3rd Parameter	1	↑	1	XX	ID2 [7:0]								XX
4th Parameter	1	↑	1	XX	ID3 [7:0]								XX
Description	This read byte returns 24 bits display identification information. The 1st parameter is dummy data. The 2nd parameter (ID1 [7:0]): LCD module's manufacturer ID. The 3rd parameter (ID2 [7:0]): LCD module/driver version ID. The 4th parameter (ID3 [7:0]): LCD module/driver ID.												
Restriction													

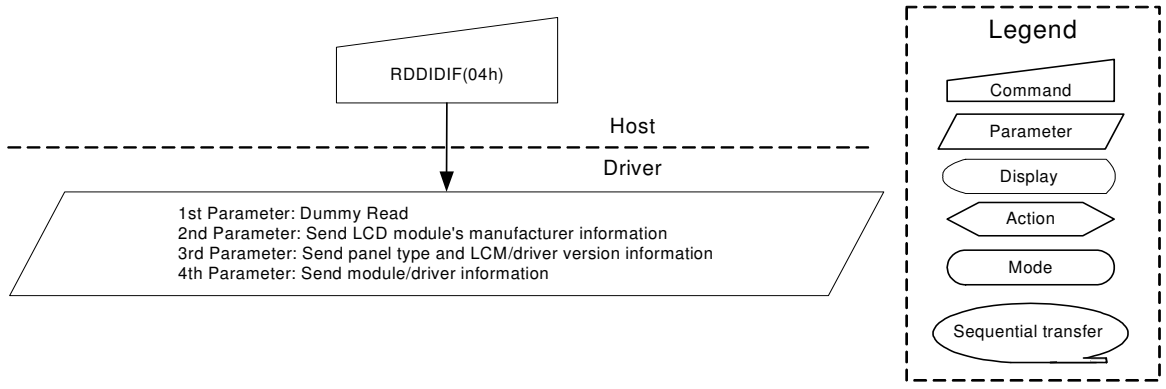
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	See description
SW Reset	See description
HW Reset	See description

Flow Chart



8.2.4. Read Display Status (09h)

09h	RDDST (Read Display Status)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	0	0	1	09h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2ndParameter	1	↑	1	XX	D [31:25]							0	00
3rdParameter	1	↑	1	XX	0	D [22:20]			D [19:16]				61
4thParameter	1	↑	1	XX	0	0	0	0	0	D [10:8]			00
5thParameter	1	↑	1	XX	D [7:5]			0	0	0	0	0	00

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value	Status
D31	Booster voltage status	0	Booster OFF
		1	Booster ON
D30	Row address order	0	Top to Bottom (When MADCTL B7='0')
		1	Bottom to Top (When MADCTL B7='1')
D29	Column address order	0	Left to Right (When MADCTL B6='0').
		1	Right to Left (When MADCTL B6='1').
D28	Row/column exchange	0	Normal Mode (When MADCTL B5='0').
		1	Reverse Mode (When MADCTL B5='1').
D27	Vertical refresh	0	LCD Refresh Top to Bottom (When MADCTL B4='0')
		1	LCD Refresh Bottom to Top (When MADCTL B4='1').
D26	RGB/BGR order	0	RGB (When MADCTL B3='0')
		1	BGR (When MADCTL B3='1')
D25	Horizontal refresh order	0	LCD Refresh Left to Right (When MADCTL B2='0')
		1	LCD Refresh Right to Left (When MADCTL B2='1')
D24	Not used	0	---
D23	Not used	0	---
D22	Interface color pixel format definition	101	16-bit/pixel
D21		110	18-bit/pixel
D20			
D19	Idle mode ON/OFF	0	Idle Mode OFF
		1	Idle Mode ON
D18	Partial mode ON/OFF	0	Partial Mode OFF
		1	Partial Mode ON.
D17	Sleep IN/OUT	0	Sleep IN Mode
		1	Sleep OUT Mode.
D16	Display normal mode ON/OFF	0	Display Normal Mode OFF.
		1	Display Normal Mode ON.
D15	Vertical scrolling status	0	Scroll OFF
D14	Not used	0	---
D13	Inversion status	0	Not defined
D12	All pixel ON	0	Not defined
D11	All pixel OFF	0	Not defined
D10	Display ON/OFF	0	Display is OFF
		1	Display is ON
D9	Tearing effect line ON/OFF	0	Tearing Effect Line OFF
		1	Tearing Effect ON
D[8:6]	Gamma curve selection	000	GC0
		001	GC1
		010	GC2
		011	GC3
		other	Not defined

	D5	Tearing effect line mode	0	Mode 1, V-Blanking only
			1	Mode 2, both H-Blanking and V-Blanking.
	D4	Not used	0	---
	D3	Not used	0	---
	D2	Not used	0	---
	D1	Not used	0	---
	D0	Not used	0	---

X = Don't care

Restriction

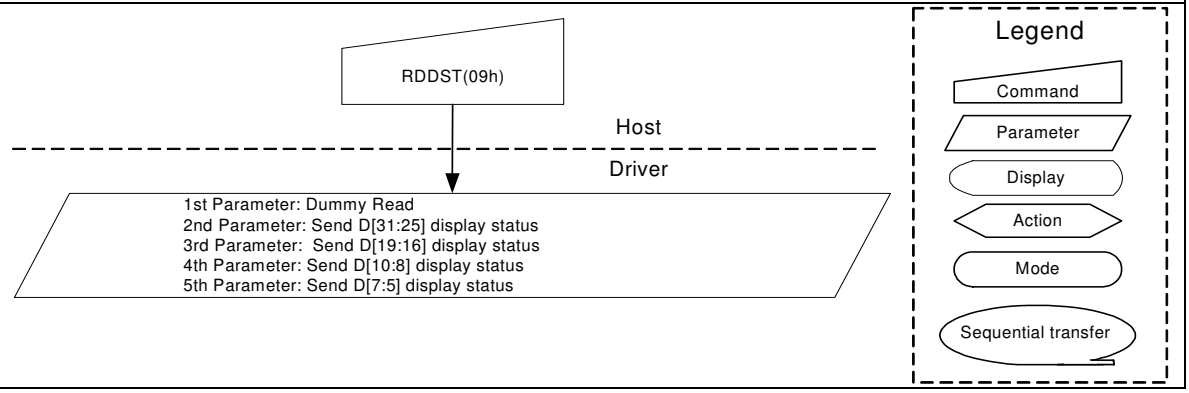
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	32'h00610000h
SW Reset	32'h00610000h
HW Reset	32'h00610000h

Flow Chart



8.2.5. Read Display Power Mode (0Ah)

0Ah	RDDPM (Read Display Power Mode)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	0	1	0	0Ah
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2ndParameter	1	↑	1	XX	D7	D6	D5	D4	D3	D2	D1	D0	08

Description

This command indicates the current status of the display as described in the table below::

Bit	Value	Description	Comment
D7	0	Booster Off or has a fault.	---
	1	Booster On and working OK	---
D6	0	Idle Mode Off.	---
	1	Idle Mode On.	---
D5	0	Partial Mode Off.	---
	1	Partial Mode On.	---
D4	0	Sleep In Mode	---
	1	Sleep Out Mode	---
D3	0	Display Normal Mode Off.	---
	1	Display Normal Mode On	---
D2	0	Display is Off.	---
	1	Display is On	---
D1	--	Not Defined	Set to '0'
D0	--	Not Defined	Set to '0'

X = Don't care

Restriction

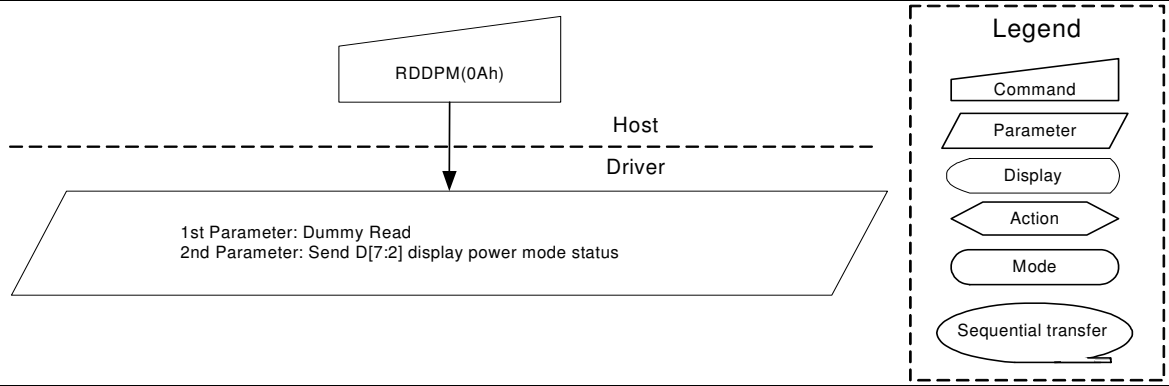
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8'h08h
SW Reset	8'h08h
HW Reset	8'h08h

Flow Chart



8.2.6. Read Display MADCTL (0Bh)

0Bh	RDDMADCTL (Read Display MADCTL)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	0	1	1	0Bh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2ndParameter	1	↑	1	XX	D7	D6	D5	D4	D3	D2	D1	D0	00

Description

This command indicates the current status of the display as described in the table below:

Bit	Value	Description	Comment
D7	0	Top to Bottom (When MADCTL B7='0').	---
	1	Bottom to Top (When MADCTL B7='1').	---
D6	0	Left to Right (When MADCTL B6='0')	---
	1	Right to Left (When MADCTL B6='1')	---
D5	0	Normal Mode (When MADCTL B5='0').	---
	1	Reverse Mode (When MADCTL B5='1')	---
D4	0	LCD Refresh Top to Bottom (When MADCTL B4='0')	---
	1	LCD Refresh Bottom to Top (When MADCTL B4='1').	---
D3	0	RGB (When MADCTL B3='0')	---
	1	BGR (When MADCTL B3='1').	---
D2	0	LCD Refresh Left to Right (When MADCTL B2='0').	---
	1	LCD Refresh Right to Left (When MADCTL B2='1').	---
D1	--	Switching between Segment outputs and RAM	Set to '0'
D0	--	Switching between Segment outputs and RAM	Set to '0'

X = Don't care

Restriction

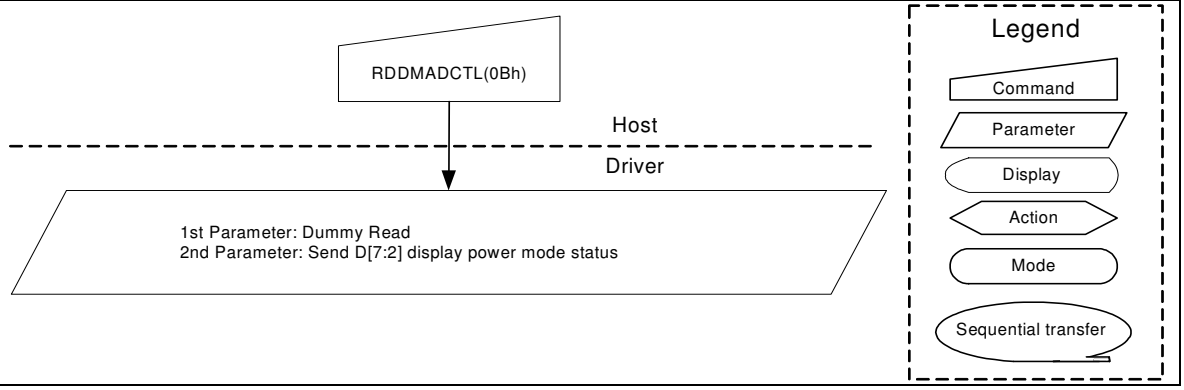
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8'h00h
SW Reset	No Change
HW Reset	8'h00h

Flow Chart



8.2.7. Read Display Pixel Format (0Ch)

0Ch	RDDCOLMOD (Read Display Pixel Format)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	1	0	0	0Ch
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	RIM	DPI [2:0]			0	DBI [2:0]			06

Description

This command indicates the current status of the display as described in the table below:

RIM	DPI [2:0]			RGB Interface Format
0	0	0	0	Reserved
0	0	0	1	Reserved
0	0	1	0	Reserved
0	0	1	1	Reserved
0	1	0	0	Reserved
0	1	0	1	16 bits / pixel
0	1	1	0	18 bits / pixel
0	1	1	1	Reserved
1	1	0	1	16 bits / pixel (6-bit 3 times data transfer)
1	1	1	0	18 bits / pixel (6-bit 3 times data transfer)

DBI [2:0]			MCU Interface Format
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	16 bits / pixel
1	1	0	18 bits / pixel
1	1	1	Reserved

X = Don't care

Restriction

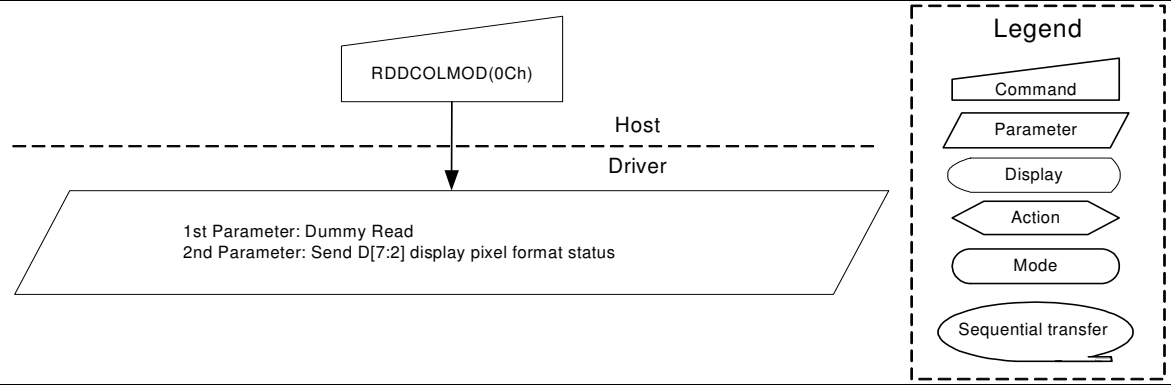
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

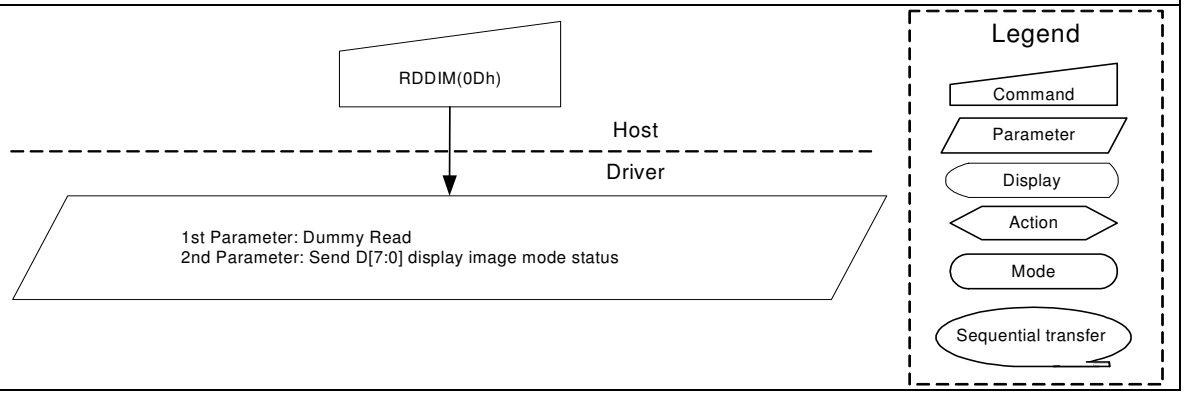
Default

Status	Default Value		
	RIM	DPI [2:0]	DBI [2:0]
Power On Sequence	1'b0	3'b000	3'b110
SW Reset	No Chang	No Chang	No Chang
HW Reset	1'b0	3'b000	3'b110

Flow Chart



8.2.8. Read Display Image Format (0Dh)

0Dh	RDDIM (Read Display Image Mode)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	1	0	1	0Dh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2ndParameter	1	↑	1	XX	0	0	0	0	0	D [2:0]			00
Description	This command indicates the current status of the display as described in the table below: D [2:0] / Description 000 / Gamma curve 1 (G2.2) 001 / Gamma curve 2 (G1.8) 010 / Gamma curve 3 (G2.5) 011 / Gamma curve 4 (G1.0) Other / Not defined X = Don't care												
Restriction													
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out / Yes Normal Mode On, Idle Mode On, Sleep Out / Yes Partial Mode On, Idle Mode Off, Sleep Out / Yes Partial Mode On, Idle Mode On, Sleep Out / Yes Sleep In / Yes												
Default	Status / Default Value Power On Sequence / 3'b000 SW Reset / 3'b000 HW Reset / 3'b000												
Flow Chart													

8.2.9. Read Display Signal Mode (0Eh)

0Eh	RDDSM (Read Display Signal Mode)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	1	1	0	0Eh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	D7	D6	D5	D4	D3	D2	D1	D0	00

Description

This command indicates the current status of the display as described in the table below:

Bit	Value	Description
D7	0	Tearing effect line OFF
	1	Tearing effect line ON
D6	0	Tearing effect line mode 1
	1	Tearing effect line mode 2
D5	0	Horizontal sync. (RGB interface) OFF
	1	Horizontal sync. (RGB interface) ON
D4	0	Vertical sync. (RGB interface) OFF
	1	Vertical sync. (RGB interface) ON
D3	0	Pixel clock (DOTCLK, RGB interface) OFF
	1	Pixel clock (DOTCLK, RGB interface) ON
D2	0	Data enable (DE, RGB interface) OFF
	1	Data enable (DE, RGB interface) ON
D1	0	Reserved
D0	0	Reserved

X = Don't care

Restriction

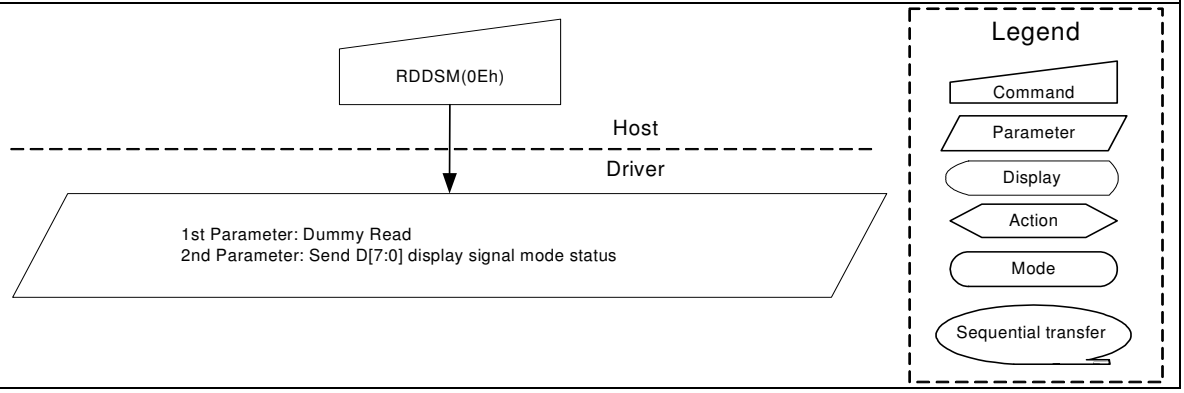
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8'h00h
SW Reset	8'h00h
HW Reset	8'h00h

Flow Chart



8.2.10. Read Display Self-Diagnostic Result (0Fh)

0Fh	RDDSDR (Read Display Self-Diagnostic Result)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	1	1	1	0Fh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	D7	D6	0	0	0	0	0	0	00

Description

Bit	Description	Action
D7	Register Loading Detection	Invert the D7 bit if register values loading work properly.
D6	Functionality Detection	Invert the D6 bit if the display is functionality
D5	Not Used	'0'
D4	Not Used	'0'
D3	Not Used	'0'
D2	Not Used	'0'
D1	Not Used	'0'
D0	Not Used	'0'

Restriction

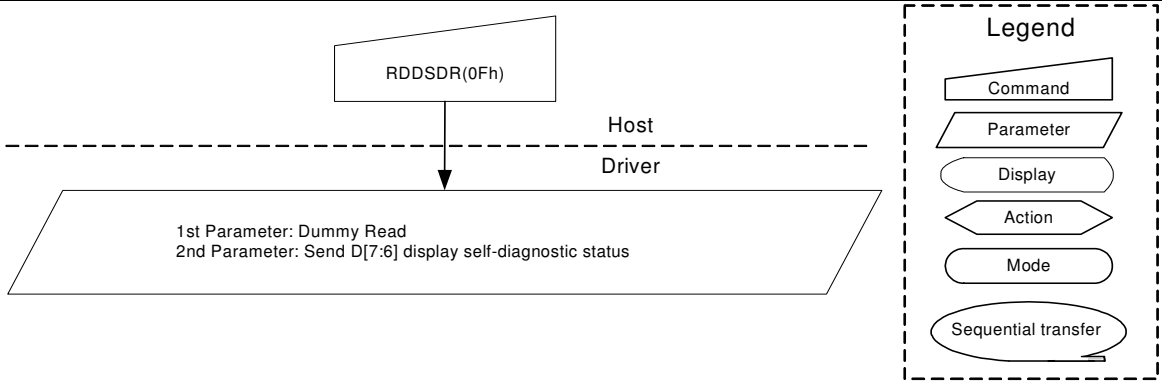
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8'h00h
SW Reset	8'h00h
HW Reset	8'h00h

Flow Chart



8.2.11. Enter Sleep Mode (10h)

10h	SPLIN (Enter Sleep Mode)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	1	0	0	0	0	10h
Parameter	No Parameter												
Description	This command causes the LCD module to enter the minimum power consumption mode. In this mode e.g. the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped. Out → Blank → STOP MCU interface and memory are still working and the memory keeps its contents. X = Don't care												
Restriction	This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h). It will be necessary to wait 5msec before sending next to command, this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.												

Register Availability

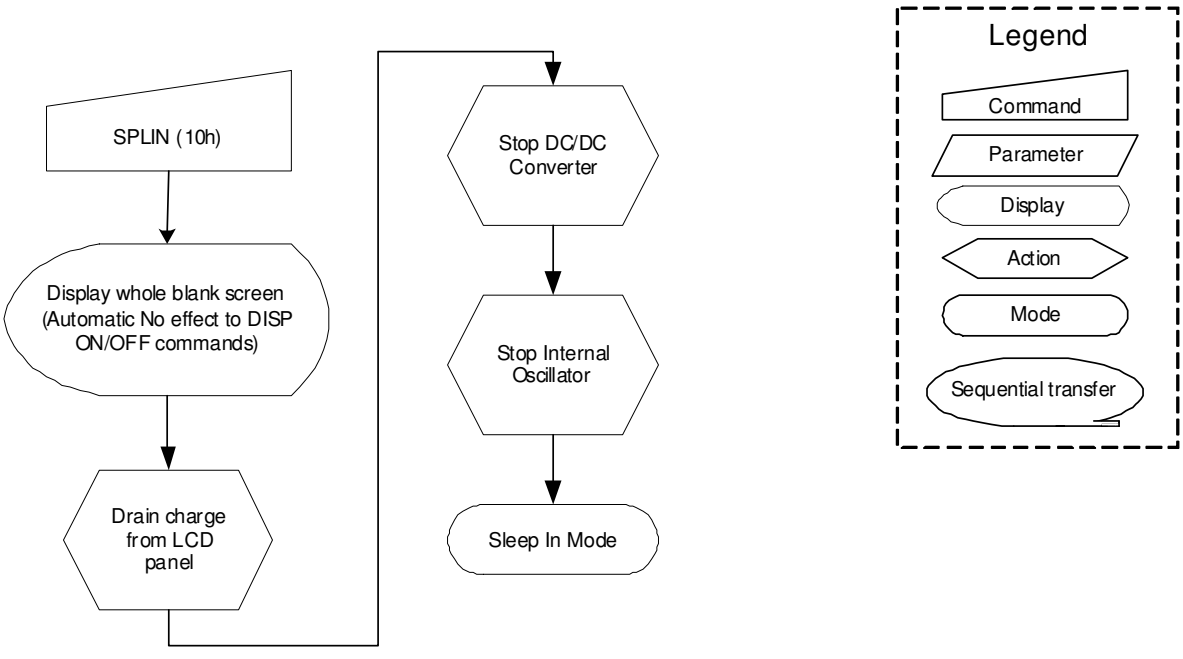
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

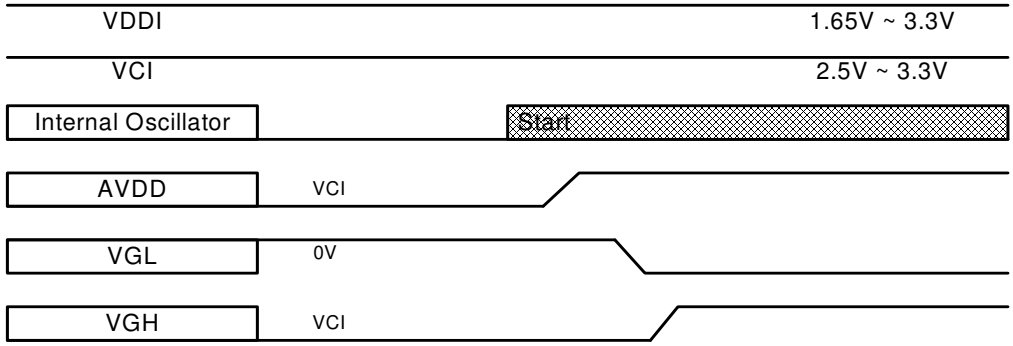
Status	Default Value
Power On Sequence	Sleep IN Mode
SW Reset	Sleep IN Mode
HW Reset	Sleep IN Mode

Flow Chart

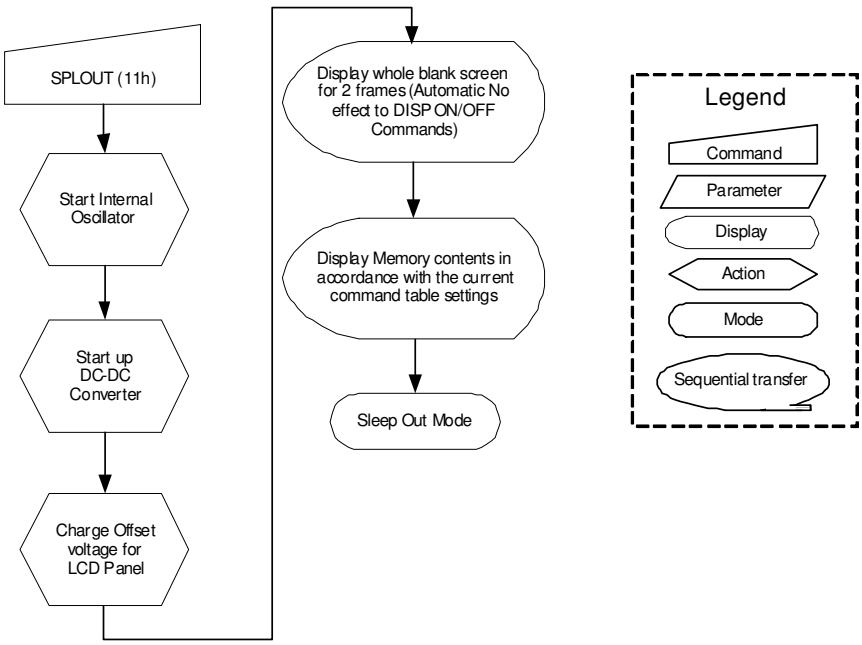
It takes 120msec to get into Sleep In mode after SLPIN command issued.



8.2.12. Sleep Out (11h)

<table>
<tr><th>11h</th><th colspan="12">SLPOUT (Sleep Out)</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>11h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command turns off sleep mode.
In this mode e.g. the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started.
 

X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h). It will be necessary to wait 5msec before sending next command, this is to allow time for the clock circuits stabilize. The display module loads all display supplier’s factory default values to the registers during this 120msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode. The display module is doing self-diagnostic functions during this 5msec. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Sleep IN Mode</td></tr><tr><td>SW Reset</td><td>Sleep IN Mode</td></tr><tr><td>HW Reset</td><td>Sleep IN Mode</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">It takes 120msec to become Sleep Out mode after SLPOUT command issued.</td></tr>
</table>



8.2.13. Partial Mode ON (12h)

<table>
<tr><th>12h</th><th colspan="12">PTLON (Partial Mode On)</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>12h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command turns on partial mode The partial mode window is described by the Partial Area command (30H). To leave Partial mode, the Normal Display Mode On command (13H) should be written.
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Partial mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Display Mode ON</td></tr><tr><td>SW Reset</td><td>Normal Display Mode ON</td></tr><tr><td>HW Reset</td><td>Normal Display Mode ON</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">See Partial Area (30h)</td></tr>
</table>

8.2.14. Normal Display Mode ON (13h)

13h	NORON (Normal Display Mode On)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	1	0	0	1	1	13h
Parameter	No Parameter												
Description	This command returns the display to normal mode. Normal display mode on means Partial mode off. Exit from NORON by the Partial mode On command (12h) X = Don't care												
Restriction	This command has no effect when Normal Display mode is active.												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Normal Display Mode ON
SW Reset	Normal Display Mode ON
HW Reset	Normal Display Mode ON

Flow Chart	See Partial Area (30h)

8.2.15. Display Inversion OFF (20h)

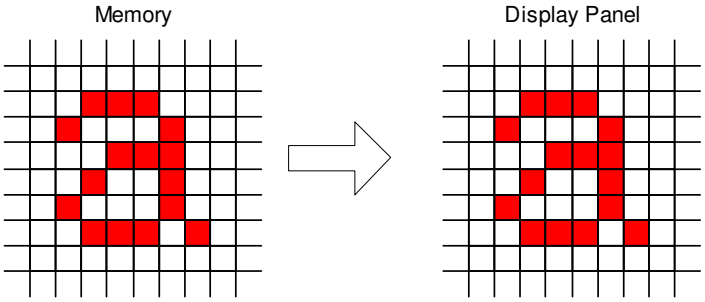
20h	DINVOFF (Display Inversion OFF)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	0	0	0	0	20h
Parameter	No Parameter												

Description

This command is used to recover from display inversion mode.

This command makes no change of the content of frame memory.

This command doesn't change any other status.



X = Don't care

Restriction

This command has no effect when module already is inversion OFF mode.

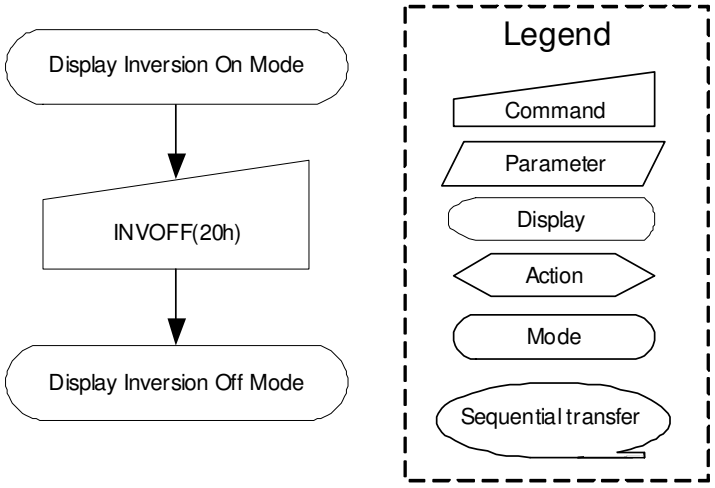
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion OFF
SW Reset	Display Inversion OFF
HW Reset	Display Inversion OFF

Flow Chart



8.2.16. Display Inversion ON (21h)

21h	DINVON (Display Inversion ON)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	0	0	0	1	21h
Parameter	No Parameter												

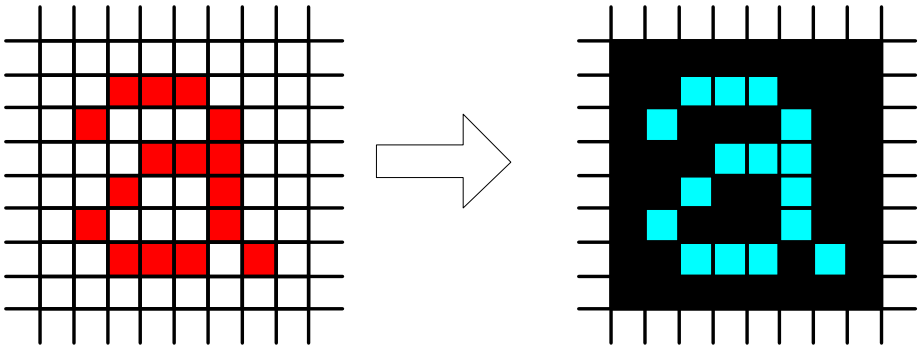
Description

This command is used to enter into display inversion mode.

This command makes no change of the content of frame memory. Every bit is inverted from the frame memory to the display.

This command doesn't change any other status.

To exit Display inversion mode, the Display inversion OFF command (20h) should be written.



X = Don't care

Restriction

This command has no effect when module already is inversion ON mode.

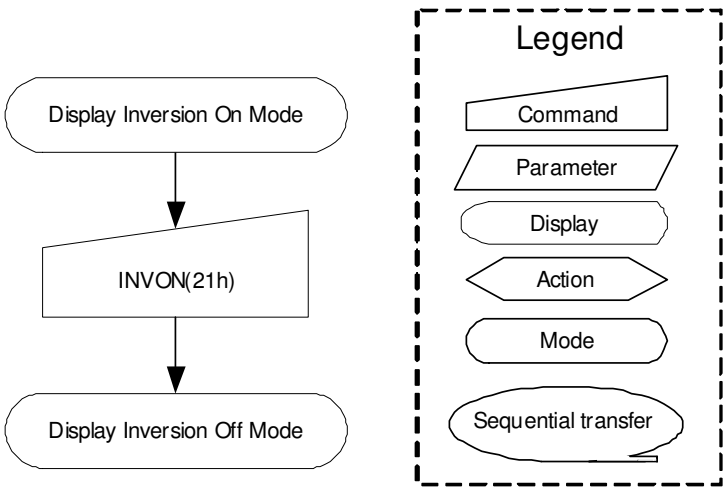
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion OFF
SW Reset	Display Inversion OFF
HW Reset	Display Inversion OFF

Flow Chart



8.2.17. Gamma Set (26h)

26h	GAMSET (Gamma Set)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	0	1	1	0	26h
Parameter	1	1	↑	XX	GC [7:0]								01

Description

This command is used to select the desired Gamma curve for the current display. A maximum of 4 fixed gamma curves can be selected. The curve is selected by setting the appropriate bit in the parameter as described in the Table:

GC [7:0]	Curve Selected
01h	Gamma curve 1 (G2.2)
02h	Gamma curve 2 (G1.8)
04h	Gamma curve 3 (G2.5)
08h	Gamma curve 4 (G1.0)

Note: All other values are undefined.

X = Don't care

Restriction

Values of GC [7:0] not shown in table above are invalid and will not change the current selected Gamma curve until valid value is received.

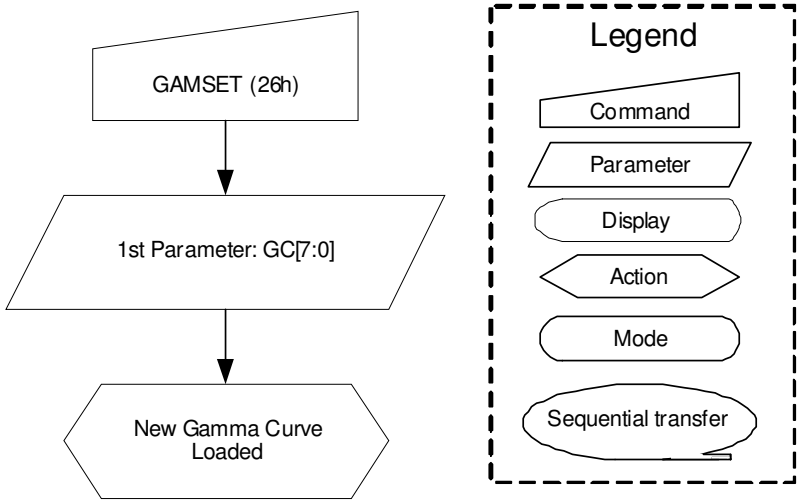
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

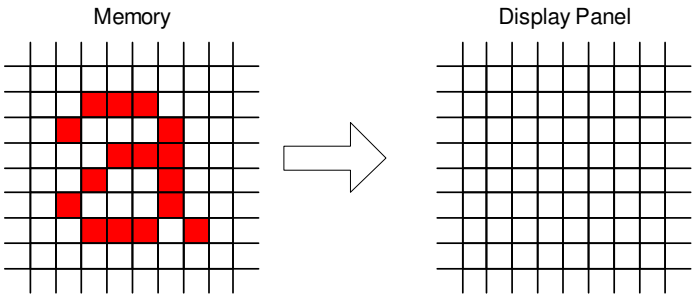
Default

Status	Default Value
Power On Sequence	8'h01h
SW Reset	8'h01h
HW Reset	8'h01h

Flow Chart



8.2.18. Display OFF (28h)

28h	DISPOFF (Display OFF)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	0	0	0	28h
Parameter	No Parameter												
Description	This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted. This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display.  X = Don't care.												
Restriction	This command has no effect when module is already in display off mode.												

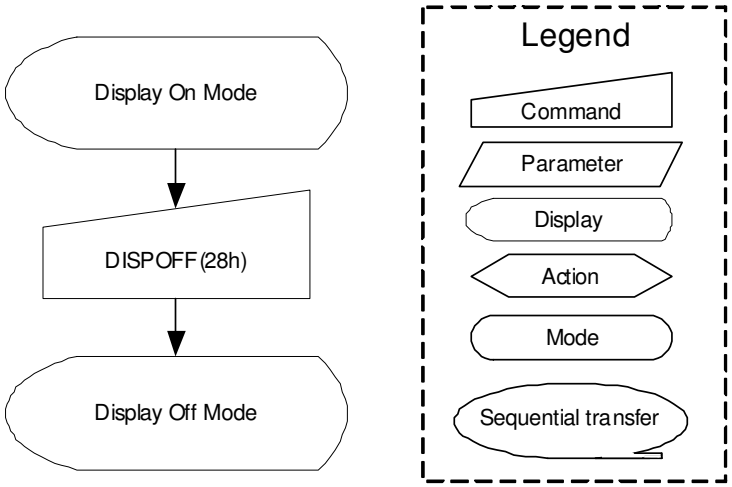
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

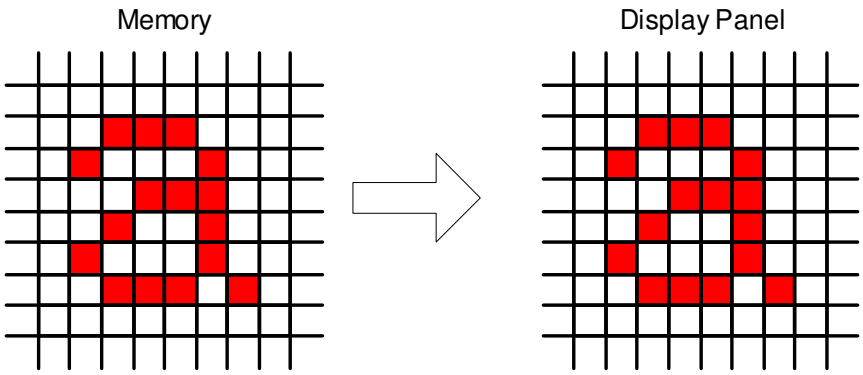
Default

Status	Default Value
Power On Sequence	Display OFF
SW Reset	Display OFF
HW Reset	Display OFF

Flow Chart



8.2.19. Display ON (29h)

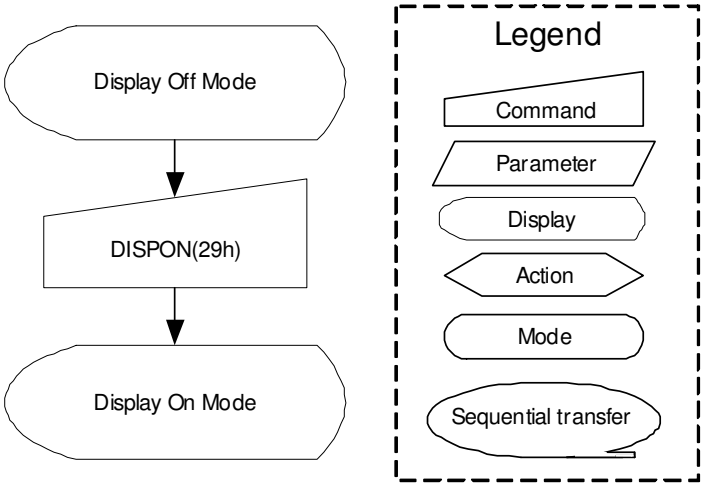
29h	DISPON (Display ON)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	0	0	1	29h
Parameter	No Parameter												
Description	This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled. This command makes no change of contents of frame memory. This command does not change any other status  X = Don't care.												
Restriction	This command has no effect when module is already in display on mode.												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display OFF
SW Reset	Display OFF
HW Reset	Display OFF

Flow Chart

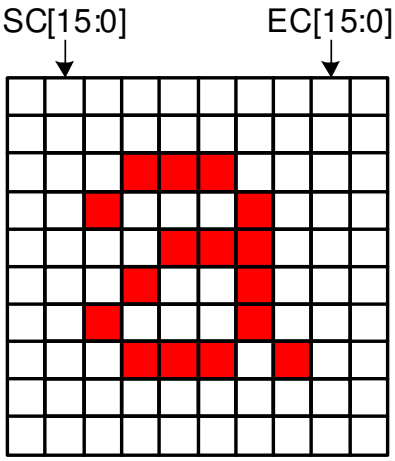


8.2.20. Column Address Set (2Ah)

2Ah	CASET (Column Address Set)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	0	1	0	2Ah
1st Parameter	1	1	↑	XX	SC15	SC14	SC13	SC12	SC11	SC10	SC9	SC8	Note1
2ndParameter	1	1	↑	XX	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	
3rd Parameter	1	1	↑	XX	EC15	EC14	EC13	EC12	EC11	EC10	EC9	EC8	Note1
4th Parameter	1	1	↑	XX	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	

Description

This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of SC [15:0] and EC [15:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.



X = Don't care

Restriction

SC [15:0] always must be equal to or less than EC [15:0].

Note 1: When SC [15:0] or EC [15:0] is greater than 00EFh (When MADCTL's B5 = 0) or 013Fh (When MADCTL's B5 = 1), data of out of range will be ignored

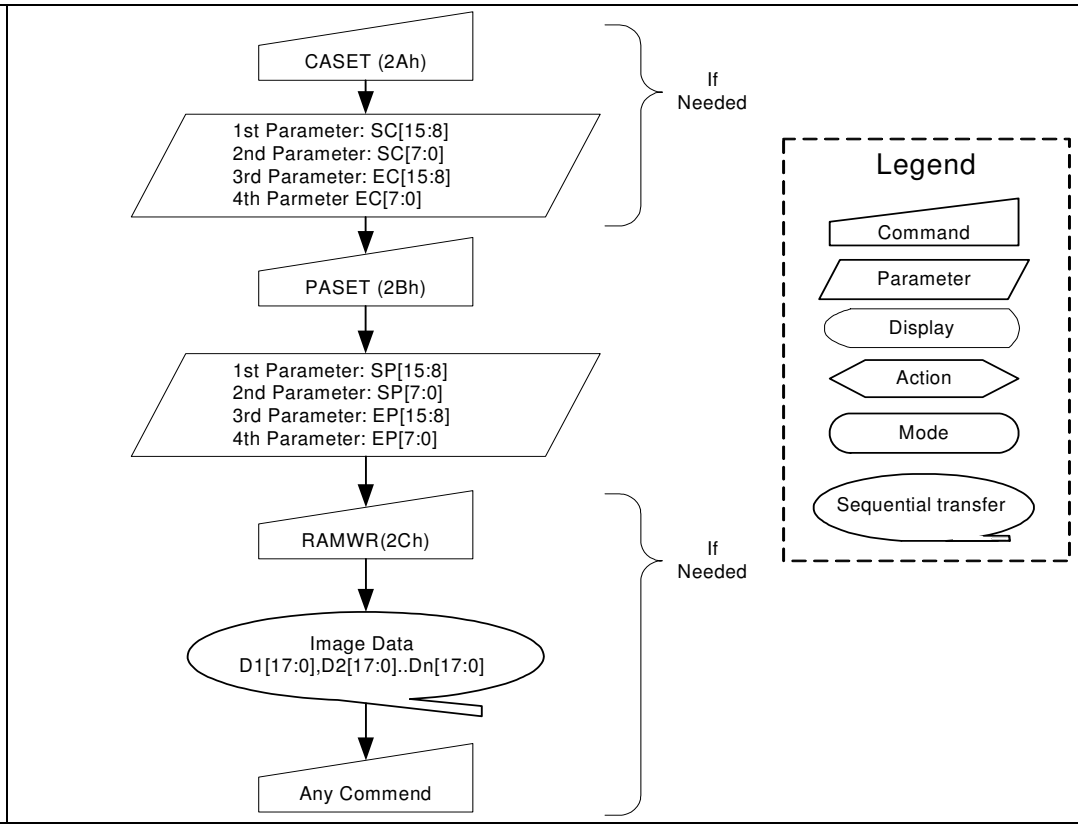
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
Power On Sequence	SC [15:0]=0000h	EC [15:0]=00EFh
SW Reset	SC [15:0]=0000h	If MADCTL's B5 = 0: EC [15:0]=00EFh If MADCTL's B5 = 1: EC [15:0]=013Fh
HW Reset	SC [15:0]=0000h	EC [15:0]=00EFh

Flow Chart

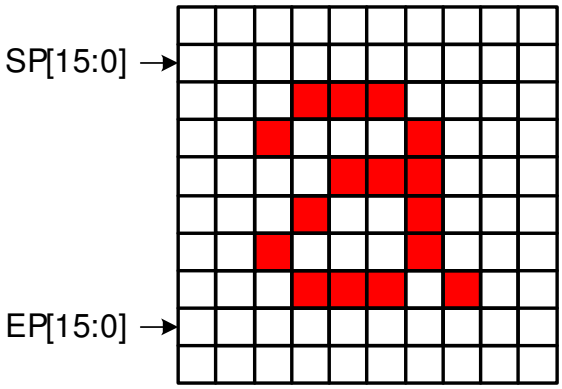


8.2.21. Page Address Set (2Bh)

2Bh	PASET (Page Address Set)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	0	1	1	2Bh
1st Parameter	1	1	↑	XX	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	Note1
2ndParameter	1	1	↑	XX	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	
3rdParameter	1	1	↑	XX	EP15	EP14	EP13	EP12	EP11	EP10	EP9	EP8	Note1
4th Parameter	1	1	↑	XX	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0	

Description

This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of SP [15:0] and EP [15:0] are referred when RAMWR command comes. Each value represents one Page line in the Frame Memory.



X = Don't care

Restriction

SP [15:0] always must be equal to or less than EP [15:0]

Note 1: When SP [15:0] or EP [15:0] is greater than 013Fh (When MADCTL's B5 = 0) or 00EFh (When MADCTL's B5 = 1), data of out of range will be ignored.

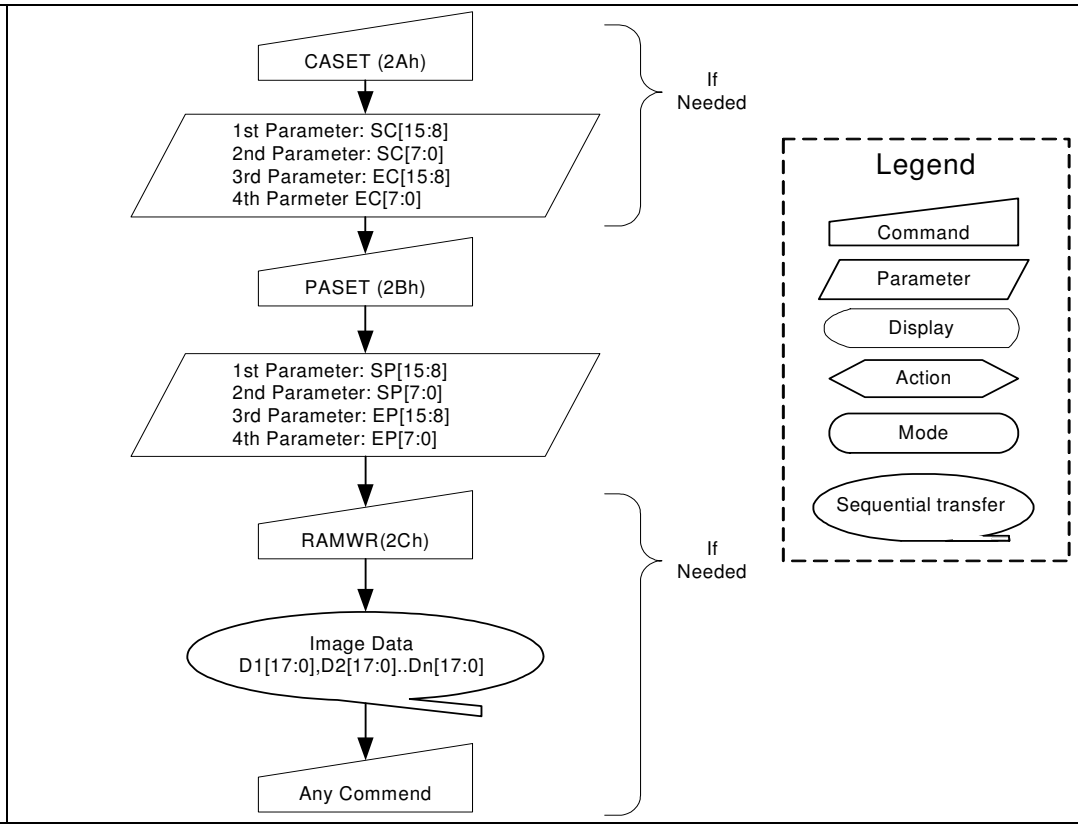
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
Power On Sequence	SP [15:0]=0000h	EP [15:0]=013Fh
SW Reset	SP [15:0]=0000h	If MADCTL's B5 = 0: EP [15:0]=013Fh If MADCTL's B5 = 1: EP [15:0]=00EFh
HW Reset	SP [15:0]=0000h	EP [15:0]=013Fh

Flow Chart



8.2.22. Memory Write (2Ch)

2Ch	RAMWR (Memory Write)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	1	0	0	2Ch
1st Parameter	1	1	↑	D1 [17:0]									XX
:	1	1	↑	Dx [17:0]									XX
Nth Parameter	1	1	↑	Dn [17:0]									XX

Description

This command is used to transfer data from MCU to frame memory. This command makes no change to the other driver status. When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions. The Start Column/Start Page positions are different in accordance with MADCTL setting.) Then D [17:0] is stored in frame memory and the column register and the page register incremented. Sending any other command can stop frame Write. X = Don't care.

Restriction

In all color modes, there is no restriction on length of parameters.

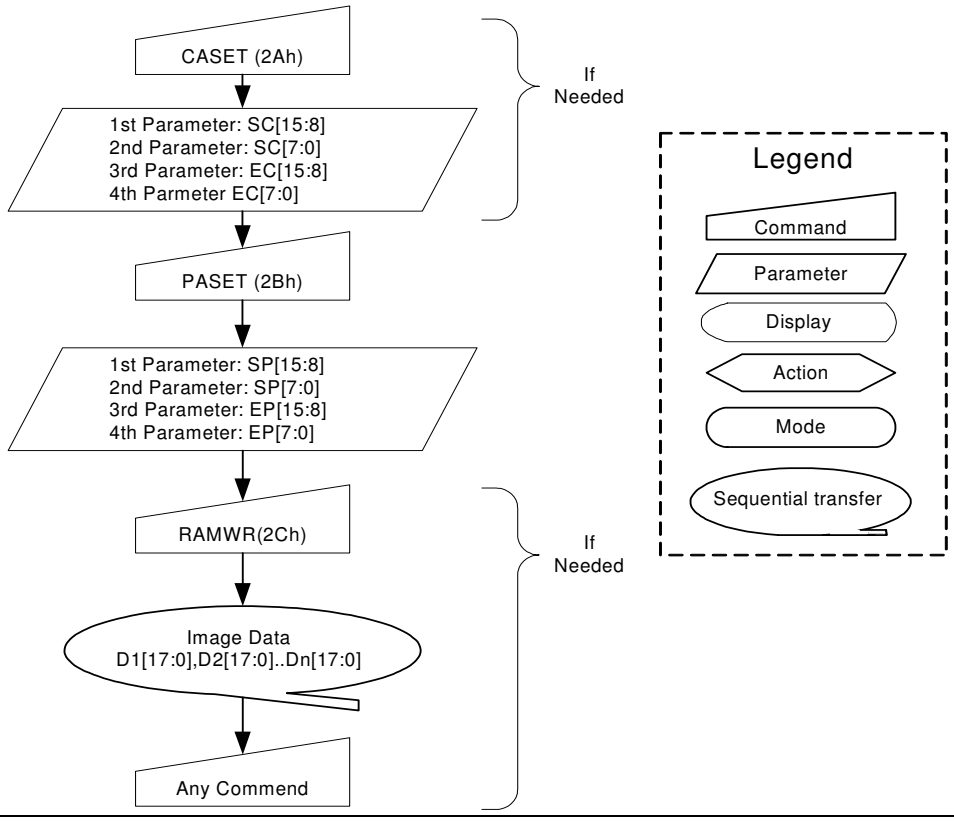
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is not cleared
HW Reset	Contents of memory is not cleared

Flow Chart



8.2.23. Color Set (2Dh)

2Dh	RGBSET (Color Set)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	1	0	1	2Dh
1st Parameter	1	1	↑	XX	R00 [5:0]								XX
nth Parameter	1	1	↑	XX	Rnn [5:0]								XX
32ndParameter	1	1	↑	XX	R31 [5:0]								XX
33rdParameter	1	1	↑	XX	G00 [5:0]								XX
nth Parameter	1	1	↑	XX	Gnn [5:0]								XX
96thParameter	1	1	↑	XX	G64 [5:0]								XX
97thParameter	1	1	↑	XX	B00 [5:0]								XX
nth Parameter	1	1	↑	XX	Bnn [5:0]								XX
128thParameter	1	1	↑	XX	B31 [5:0]								XX
Description	This command is used to define the LUT for 16-bit to 18-bit color depth conversion. 128 bytes must be written to the LUT regardless of the color mode. Only the values in Section 7.4 are referred. This command has no effect on other commands, parameter and contents of frame memory. Visible change takes effect next time the frame memory is written to.												
Restriction													

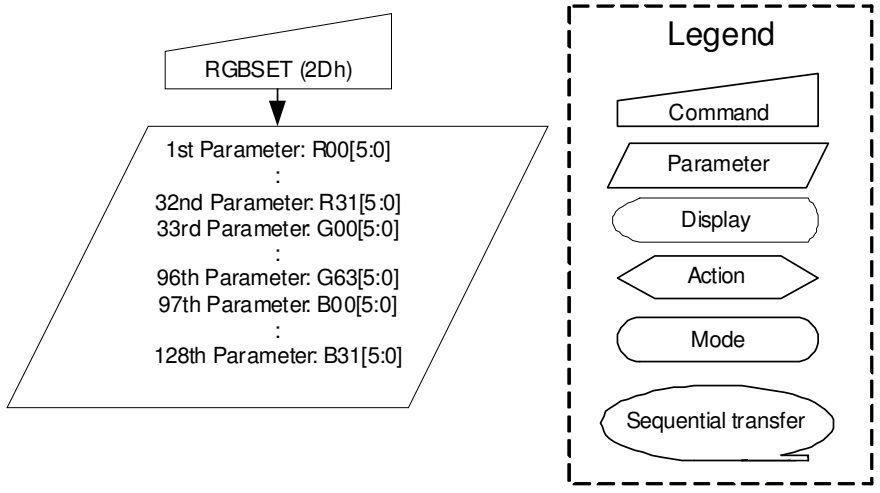
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Random values
SW Reset	Contents of LUT protected
HW Reset	Random values

Flow Chart



8.2.24. Memory Read (2Eh)

2Eh	RAMRD (Memory Read)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	1	1	0	2Eh
1st Parameter	1	1	↑	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	1	↑	D1 [17:0]									XX
:	1	1	↑	Dx [17:0]									XX
(N+1)th Parameter	1	1	↑	Dn [17:0]									XX

Description

This command transfers image data from ILI9340's frame memory to the host processor starting at the pixel location specified by preceding set_column_address and set_page_address commands.

If Memory Access control B5 = 0:

The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The column register is then incremented and pixels read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host processor sends another command.

If Memory Access Control B5 = 1:

The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The page register is then incremented and pixels read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value or the host processor sends another command.

Restriction

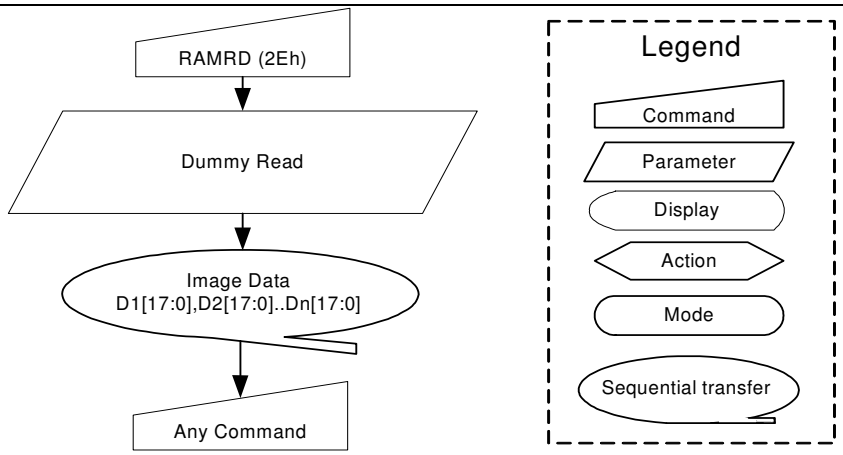
There is no restriction on length of parameters.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is set randomly
HW Reset	Contents of memory is set randomly

Flow Chart	

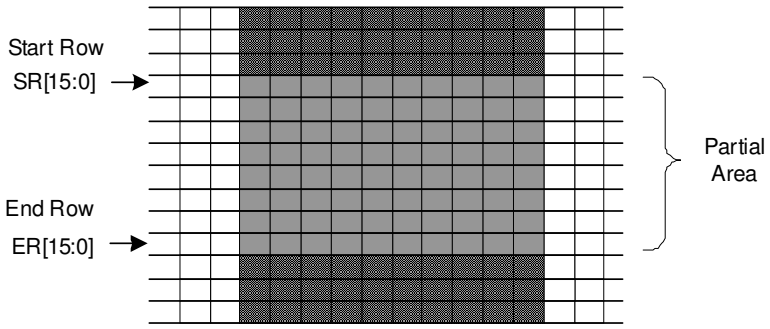
8.2.25. Partial Area (30h)

30h	PLTAR (Partial Area)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	0	0	0	30h
1st Parameter	1	1	↑	XX	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	00
2ndParameter	1	1	↑	XX	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	00
3rdParameter	1	1	↑	XX	ER15	ER14	ER13	ER12	ER11	ER10	ER9	ER8	01
4th Parameter	1	1	↑	XX	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	3F

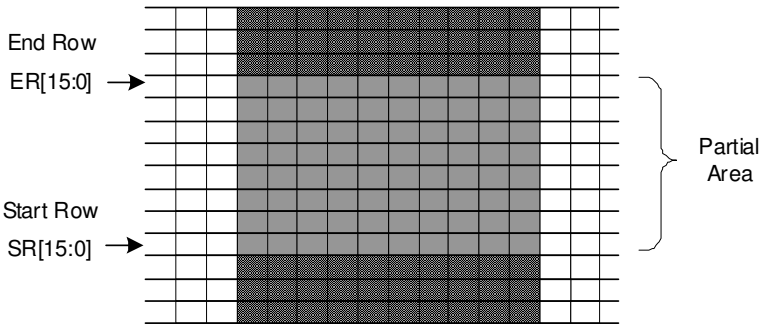
Description

This command defines the partial mode's display area. There are 2 parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer.

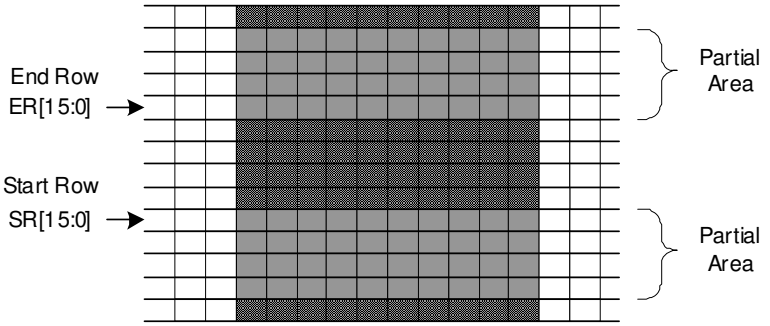
If End Row>Start Row when MADCTL B4=0:-



If End Row>Start Row when MADCTL B4=1:-



If End Row<Start Row when MADCTL B4=0:-



If End Row = Start Row then the Partial Area will be one row deep.

X = Don't care.

Restriction	SR [15…0] and ER [15…0] cannot be 0000h nor exceed 013Fh.

Register Availability

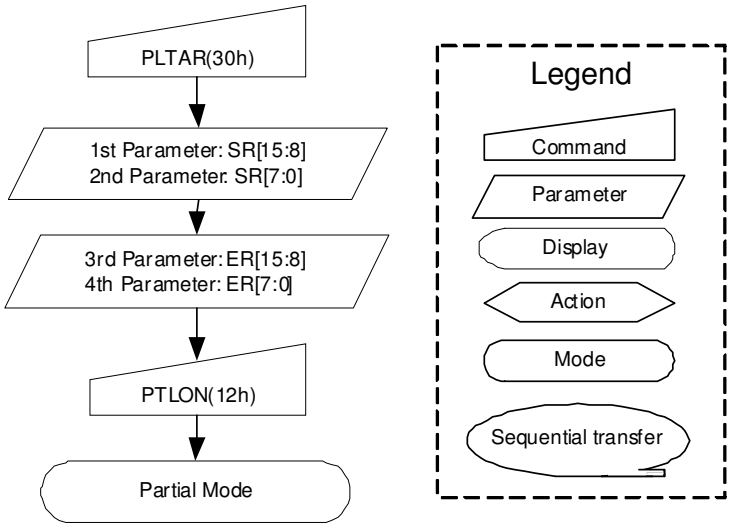
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

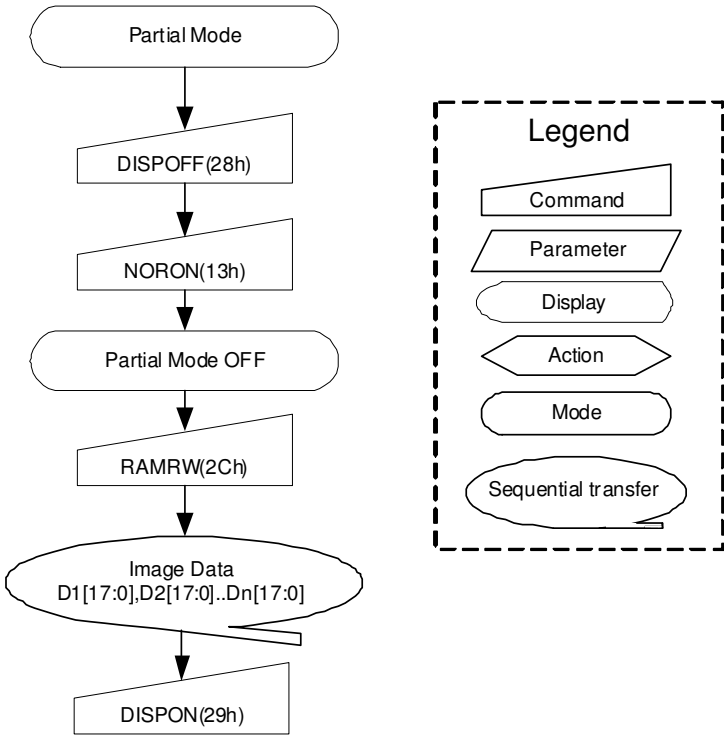
Status	Default Value	
	SR [15:0]	ER [15:0]
Power On Sequence	16'h0000h	16'h013Fh
SW Reset	16'h 0000h	16'h 013Fh
HW Reset	16'h 0000h	16'h 013Fh

Flow Chart

1. To Enter Partial Mode



2. To Leave Partial Mode



8.2.26. Vertical Scrolling Definition (33h)

33h	VSCRDEF (Vertical Scrolling Definition)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	0	1	1	33h
1st Parameter	1	↑	1	XX	TFA [15:8]								00
2nd Parameter	1	↑	1	XX	TFA [7:0]								00
3rd Parameter	1	↑	1	XX	VSA [15:8]								01
4th Parameter	1	↑	1	XX	VSA [7:0]								40
5th Parameter	1	↑	1	XX	BFA [15:8]								00
6th Parameter	1	↑	1	XX	BFA [7:0]								00

Description

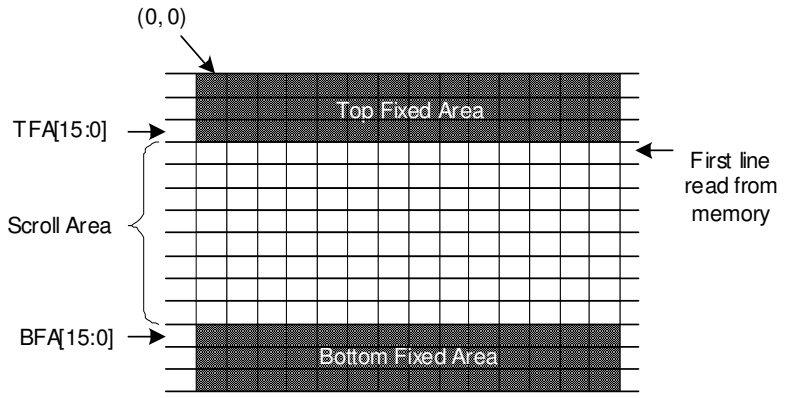
This command defines the Vertical Scrolling Area of the display.

When MADCTL B4=0

The 1st & 2nd parameter TFA [15...0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).

The 3rd & 4th parameter VSA [15...0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area.

The 5th & 6th parameter BFA [15...0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display). TFA, VSA and BFA refer to the Frame Memory Line Pointer.

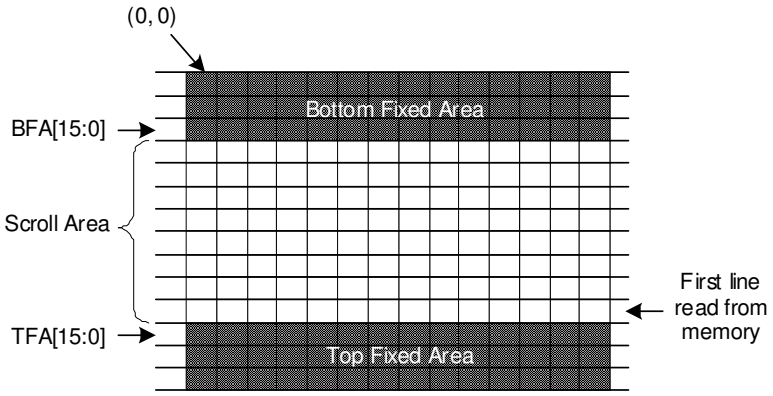


When MADCTL B4=1

The 1st & 2nd parameter TFA [15...0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).

The 3rd & 4th parameter VSA [15...0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area.

The 5th & 6th parameter BFA [15...0] describes the Bottom Fixed Area (in No. of lines from Top of the Frame Memory and Display).



X = Don't care

Restriction

Register Availability

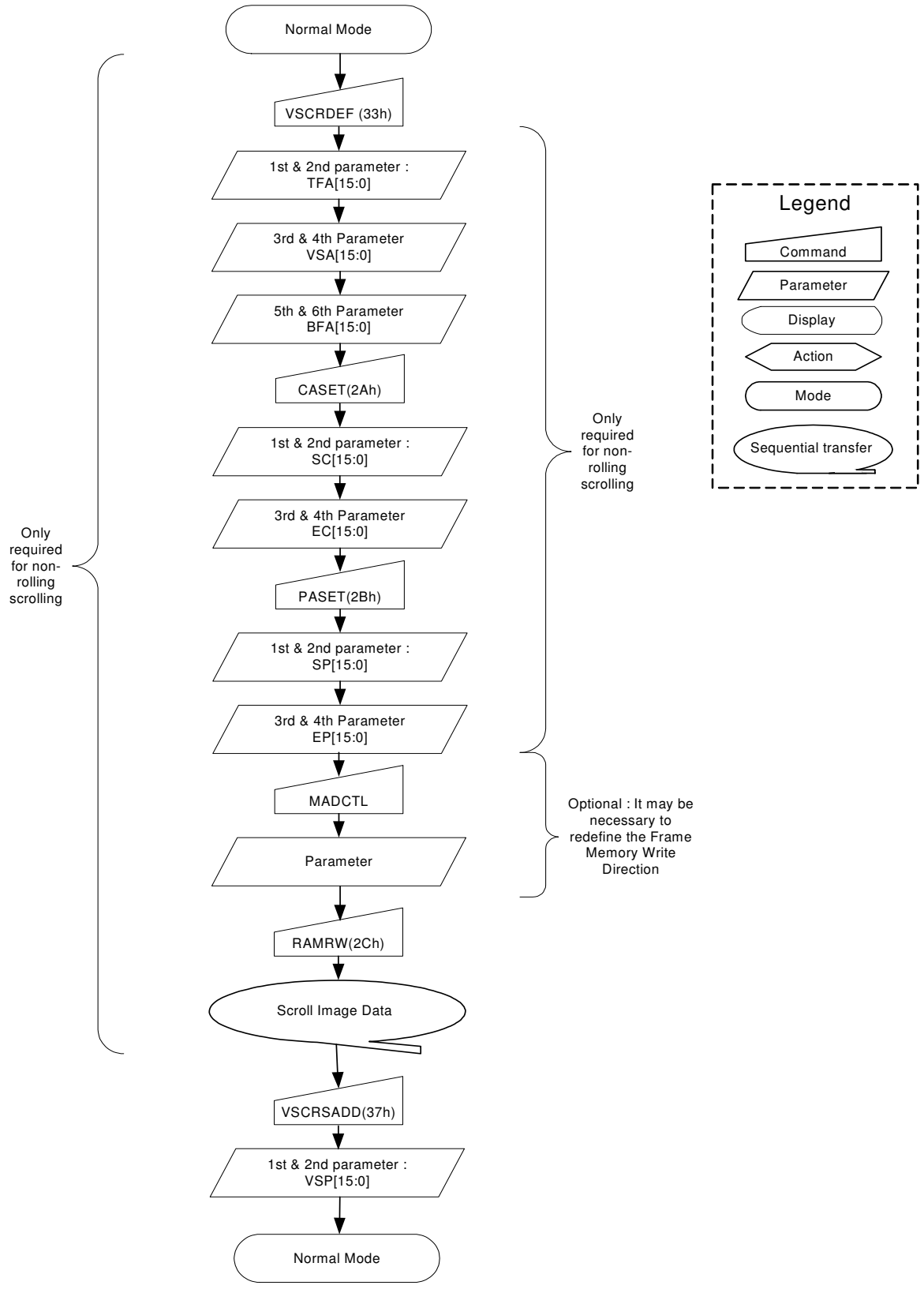
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	TFA [15:0]	VSA [15:0]	BFA [15:0]
Power On Sequence	16'h0000h	16'h0140h	16'h0000h
SW Reset	16'h0000h	16'h0140h	16'h0000h
HW Reset	16'h0000h	16'h0140h	16'h0000h

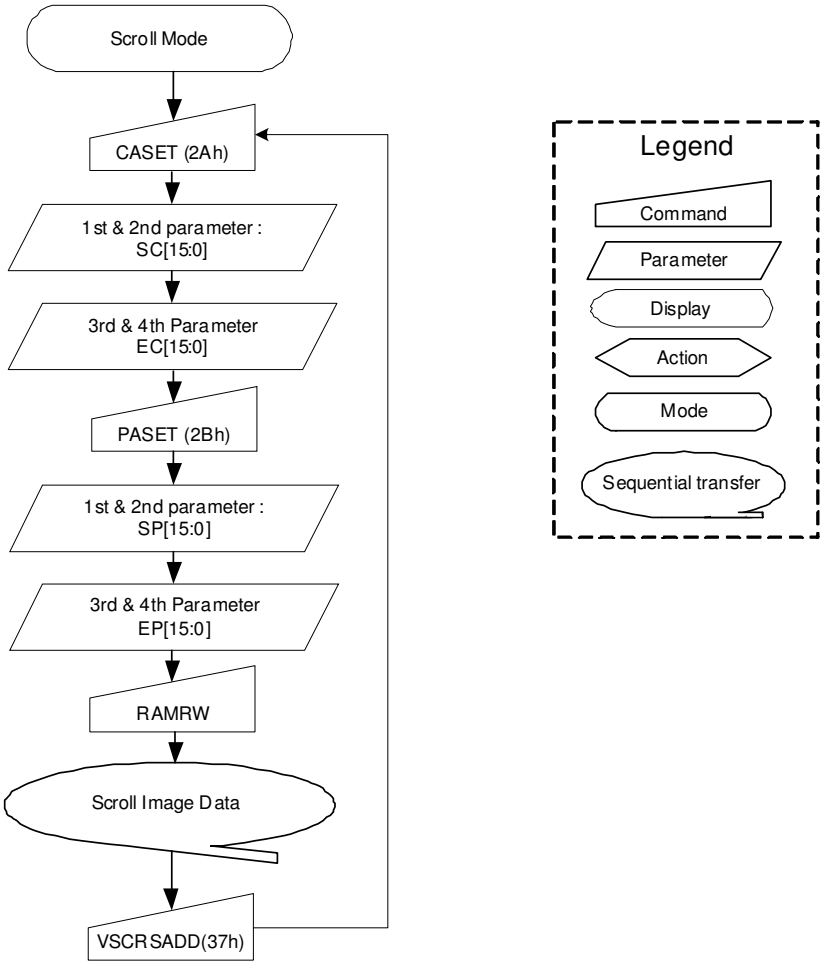
Flow Chart

1. To enter Vertical Scroll Mode :

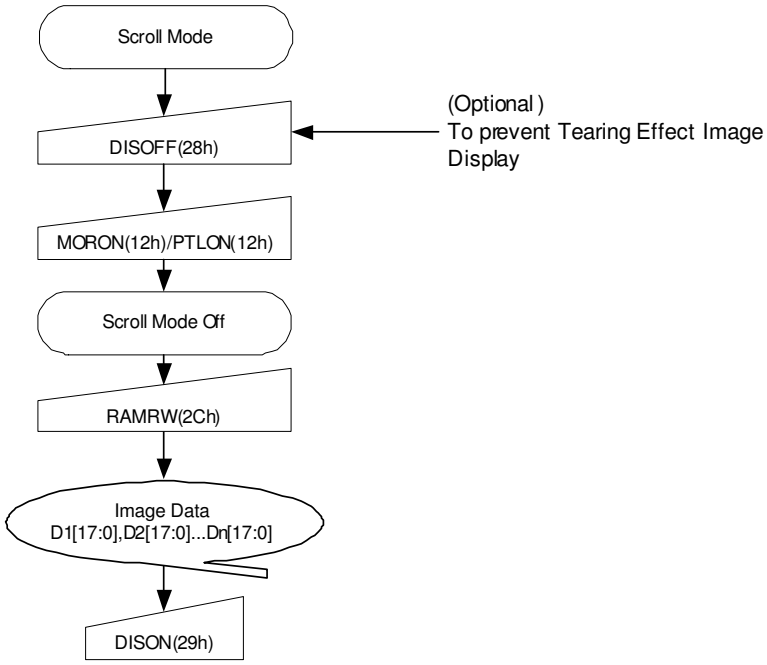


Note : The Frame Memory Window size ,must be defined correctly otherwise undesirable image will be displayed.

2. Continuous Scroll :



3.To Leave Vertical Scroll Mode:



Note: Scroll Mode can be left by both the Normal Display Mode ON (13h) and Partial Mode ON (12h) commands.

8.2.27. Tearing Effect Line OFF (34h)

34h	TEOFF (Tearing Effect Line OFF)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	1	0	0	34h
Parameter	No Parameter												
Description	This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line. X = Don't care.												
Restriction	This command has no effect when Tearing Effect output is already OFF.												

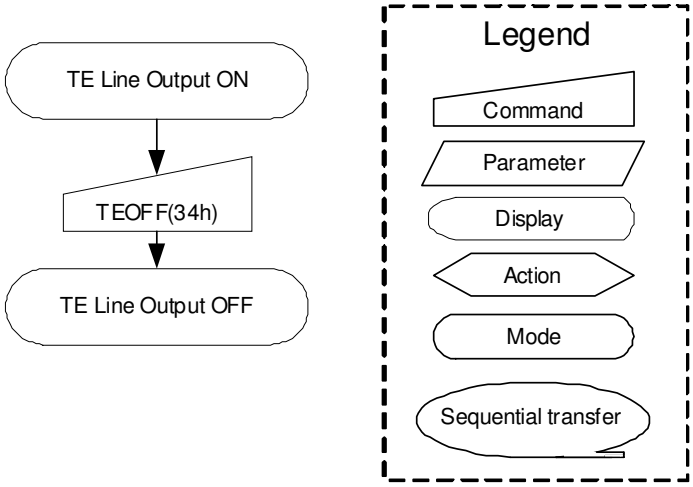
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	OFF
SW Reset	OFF
HW Reset	OFF

Flow Chart



8.2.28. Tearing Effect Line ON (35h)

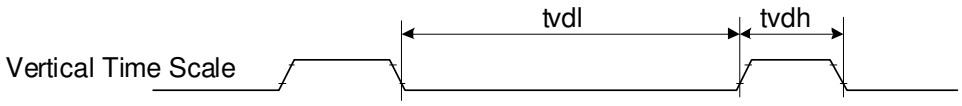
35h	TEON (Tearing Effect Line ON)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	1	0	1	35h
Parameter	1	1	↑	XX	0	0	0	0	0	0	0	M	00

Description

This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTL bit B4. The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line.

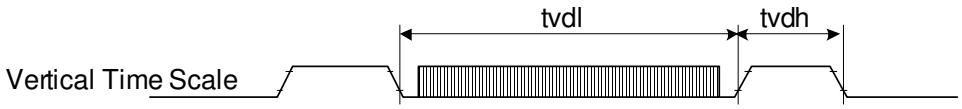
When **M=0**:

The Tearing Effect Output line consists of V-Blanking information only:



When **M=1**:

The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:



Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

X = Don't care.

Restriction

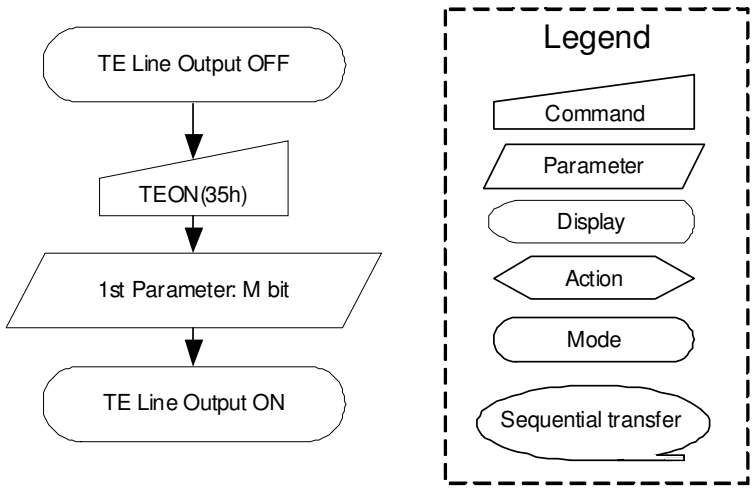
This command has no effect when Tearing Effect output is already ON

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	OFF
SW Reset	OFF
HW Reset	OFF

Flow Chart	

8.2.29. Memory Access Control (36h)

36h	MADCTL (Memory Access Control)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	1	1	0	36h
Parameter	1	1	↑	XX	MY	MX	MV	ML	BGR	MH	0	0	00

Description

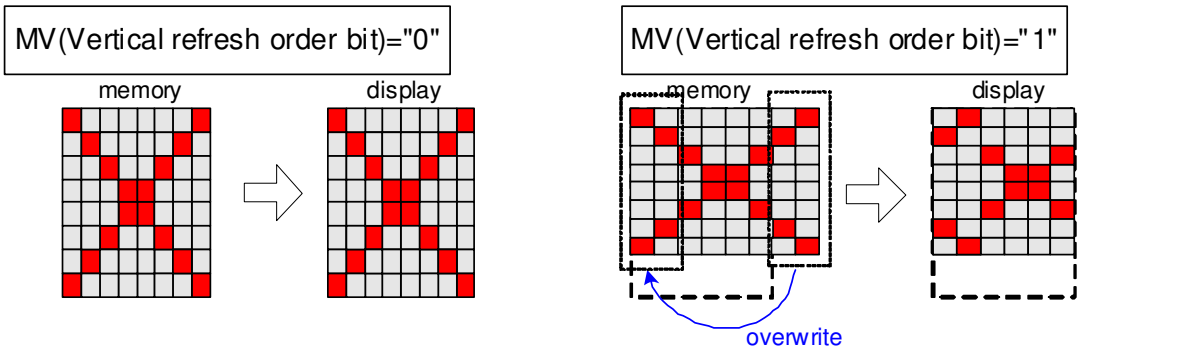
This command defines read/write scanning direction of frame memory.

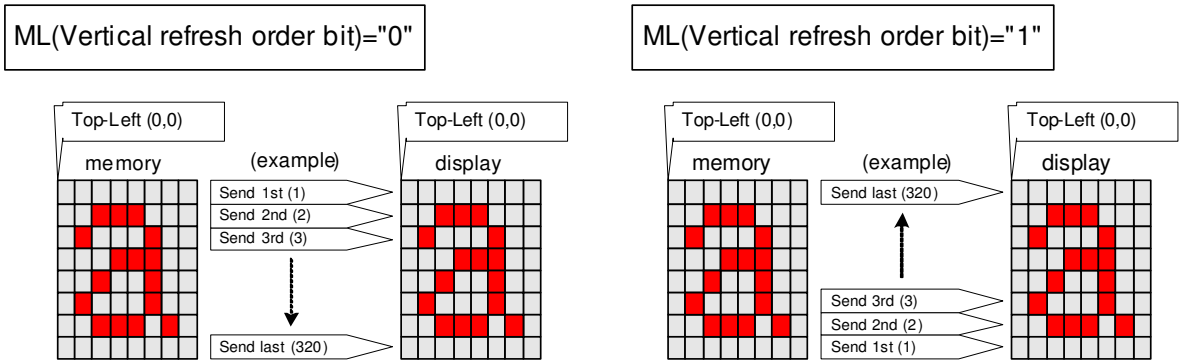
This command makes no change on the other driver status.

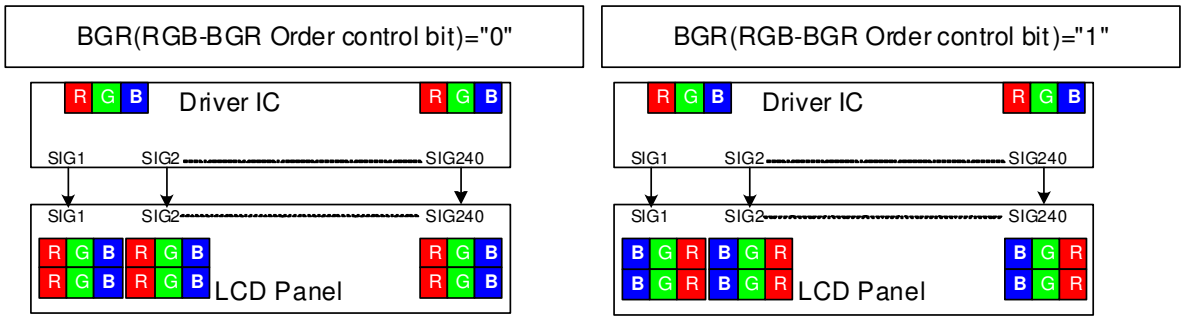
Bit	Name	Description
MY	Row Address Order	These 3 bits control MCU to memory write/read direction.
MX	Column Address Order	
MV	Row / Column Exchange	
ML	Vertical Refresh Order	LCD vertical refresh direction control.
BGR	RGB-BGR Order	Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)
MH	Horizontal Refresh ORDER	LCD horizontal refreshing direction control.

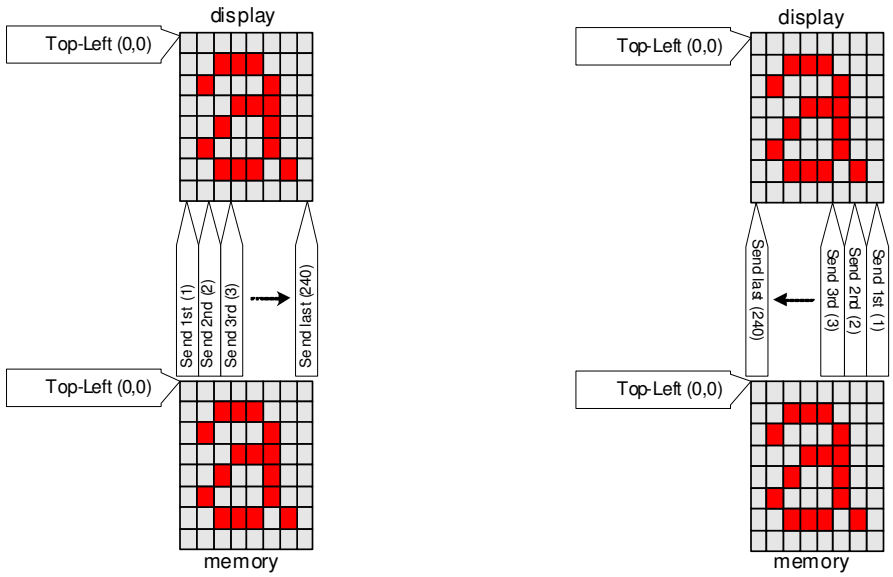
Note: When BGR bit is changed, the new setting is active immediately without update the content in Frame Memory again.

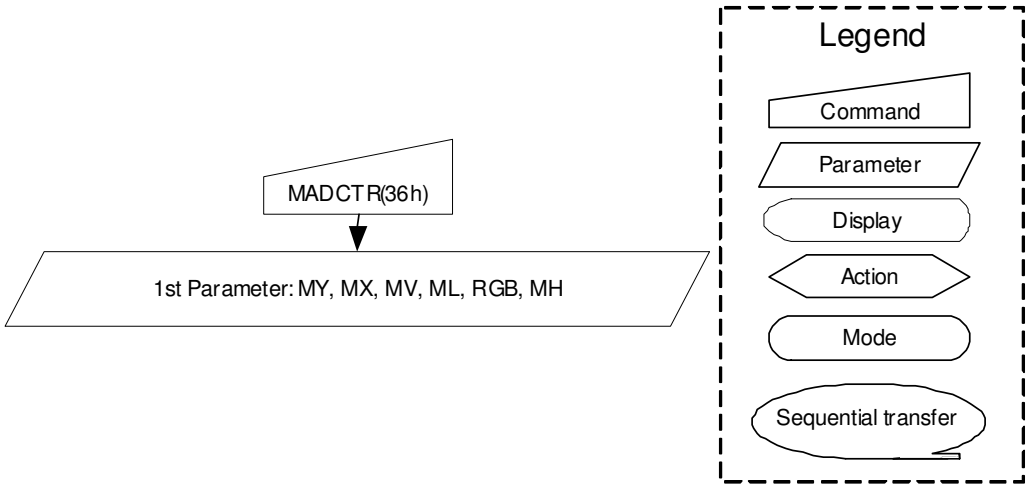
X = Don't care.







<table>
<tr><td></td><td>
MH(Horizontal refresh order control bit)="0" | MH(Horizontal refresh order control bit)="1"


Note: Top-Left (0,0) means a physical memory location.
</td></tr>
<tr><td>Restriction</td><td></td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’h00h</td></tr>
<tr><td>SW Reset</td><td>No change</td></tr>
<tr><td>HW Reset</td><td>8’h00h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>


</td></tr>
</table>

8.2.30. Vertical Scrolling Start Address (37h)

37h	VSCRSADD (Vertical Scrolling Start Address)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	1	1	1	37h
1st Parameter	1	↑	1	XX	VSP [15:8]								00
2nd Parameter	1	↑	1	XX	VSP [7:0]								00

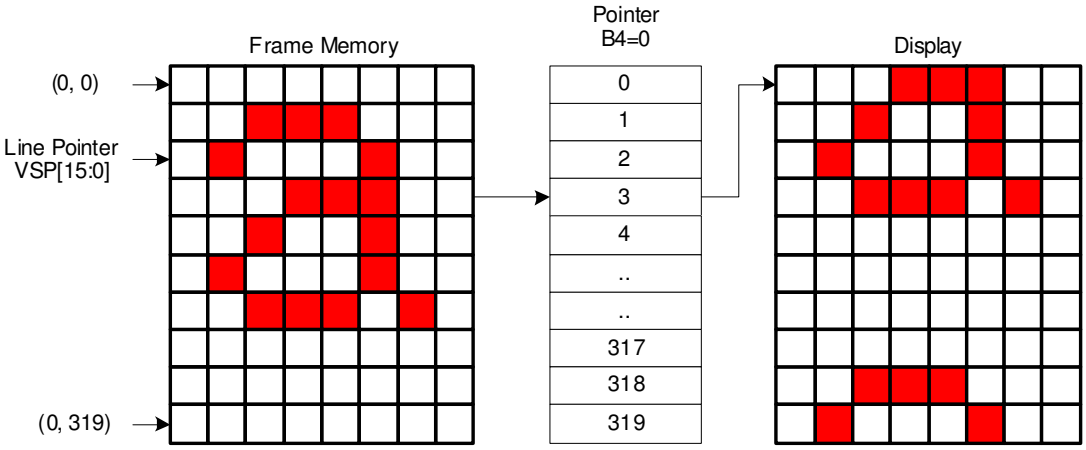
Description

This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode. The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:-

When MADCTL B4=0

Example:

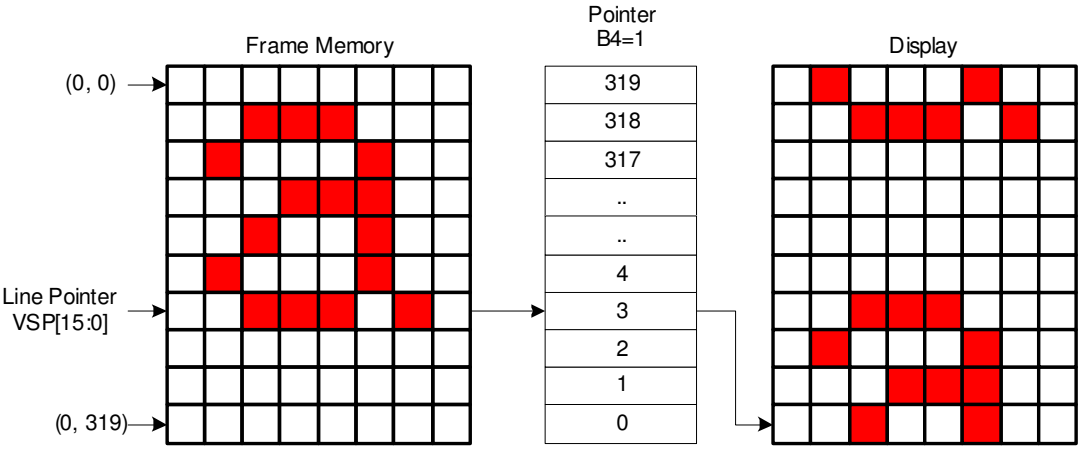
When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 320 and VSP='3'.



When MADCTL B4=1

Example:

When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 320 and VSP='3'.



Note: (1) When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect. VSP refers to the Frame Memory line Pointer.

(2) This command is ignored when the ILI9340 enters Partial mode.

X = Don't care

<table>
<tr><td>Restriction</td><td></td></tr>
<tr><td>Register
Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>No</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>No</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>VSP [15:0]</th></tr>
<tr><td>Power On Sequence</td><td>16’h0000h</td></tr>
<tr><td>SW Reset</td><td>16’h0000h</td></tr>
<tr><td>HW Reset</td><td>16’h0000h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>See Vertical Scrolling Definition (33h) description.</td></tr>
</table>

8.2.31. Idle Mode OFF (38h)

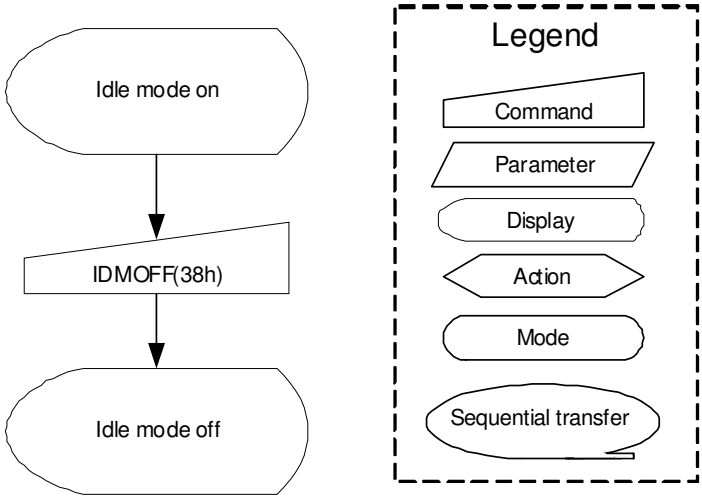
38h	IDMOFF (Idle Mode OFF)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	1	0	0	0	38h
Parameter	No Parameter												
Description	This command is used to recover from Idle mode on. In the idle off mode, LCD can display maximum 262,144 colors. X = Don't care.												
Restriction	This command has no effect when module is already in idle off mode.												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle mode OFF
SW Reset	Idle mode OFF
HW Reset	Idle mode OFF

Flow Chart



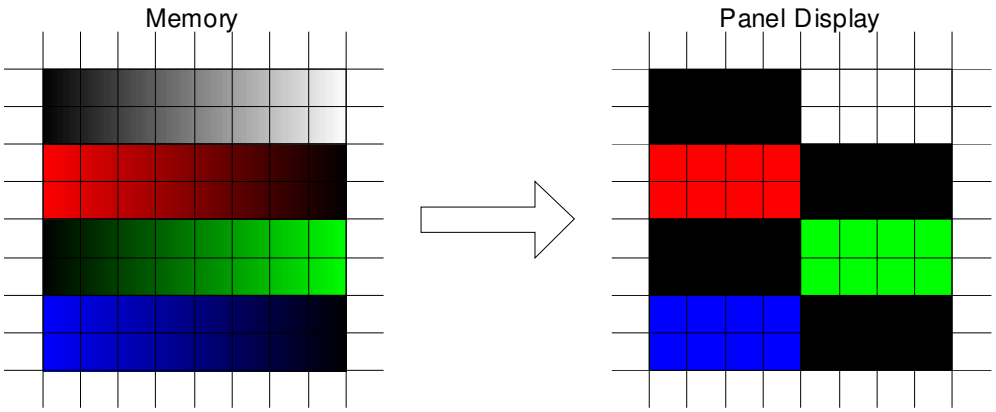
8.2.32. Idle Mode ON (39h)

39h	IDMON (Idle Mode ON)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	1	0	0	1	39h
Parameter	No Parameter												

Description

This command is used to enter into Idle mode on.

In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.



Memory Contents vs. Display Color			
	$R_5\ R_4\ R_3\ R_2\ R_1\ R_0$	$G_5\ G_4\ G_3\ G_2\ G_1\ G_0$	$B_5\ B_4\ B_3\ B_2\ B_1\ B_0$
Black	0XXXXX	0XXXXX	0XXXXX
Blue	0XXXXX	0XXXXX	1XXXXX
Red	1XXXXX	0XXXXX	0XXXXX
Magenta	1XXXXX	0XXXXX	1XXXXX
Green	0XXXXX	1XXXXX	0XXXXX
Cyan	0XXXXX	1XXXXX	1XXXXX
Yellow	1XXXXX	1XXXXX	0XXXXX
White	1XXXXX	1XXXXX	1XXXXX

X = Don't care.

Restriction

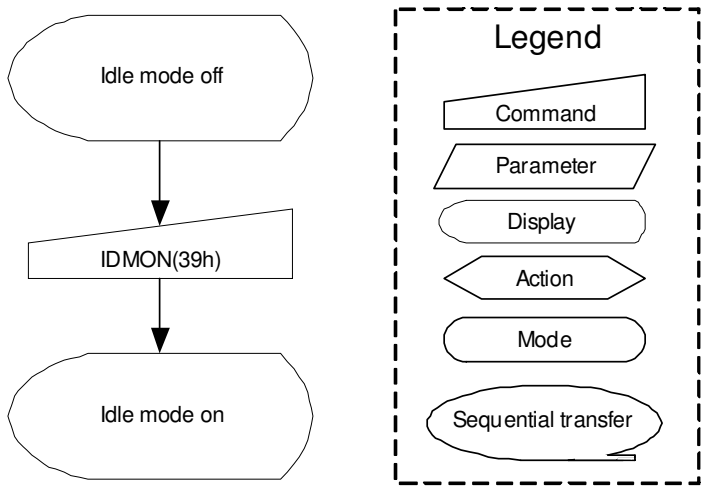
This command has no effect when module is already in idle off mode.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle mode OFF
SW Reset	Idle mode OFF
HW Reset	Idle mode OFF

Flow Chart	

8.2.33. COLMOD: Pixel Format Set (3Ah)

3Ah	PIXSET (Pixel Format Set)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	1	0	1	0	3Ah
Parameter	1	1	↑	XX	0	DPI [2:0]			0	DBI [2:0]			66

Description

This command sets the pixel format for the RGB image data used by the interface. DPI [2:0] is the pixel format select of RGB interface and DBI [2:0] is the pixel format of MCU interface. If a particular interface, either RGB interface or MCU interface, is not used then the corresponding bits in the parameter are ignored. The pixel format is shown in the table below.

DPI [2:0]			RGB Interface Format
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	16 bits / pixel
1	1	0	18 bits / pixel
1	1	1	Reserved

DBI [2:0]			MCU Interface Format
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	16 bits / pixel
1	1	0	18 bits / pixel
1	1	1	Reserved

If using RGB Interface must selection serial interface.

X = Don't care

Restriction

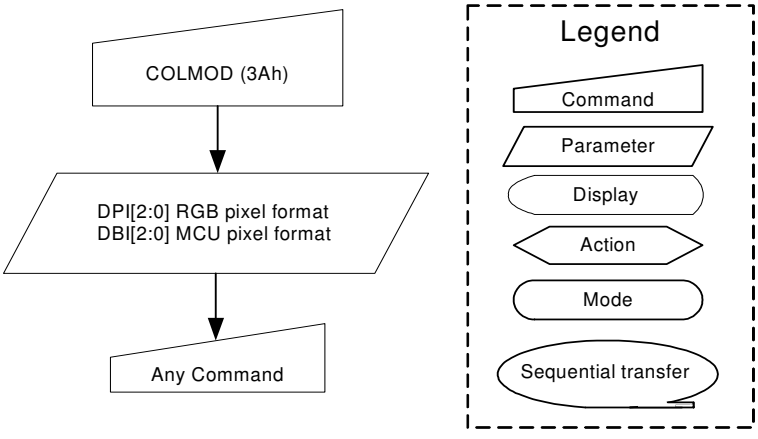
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	DPI [2:0]	DBI [2:0]
Power On Sequence	3'b110	3'b110
SW Reset	No Change	No Change
HW Reset	3'b110	3'b110

Flow Chart



8.2.34. Write_Memory_Continue (3Ch)

3Ch	Write_Memory_Continue												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	1	1	0	0	3Ch
1st Parameter	1	1	↑	D1 [17..8]	D1 [7]	D1 [6]	D1 [5]	D1 [4]	D1 [3]	D1 [2]	D1 [1]	D1 [0]	000 3FF
Xth Parameter	1	1	↑	Dx [17..8]	Dx [7]	Dx [6]	Dx [5]	Dx [4]	Dx [3]	Dx [2]	Dx [1]	Dx [0]	000 3FF
Nth Parameter	1	1	↑	Dn [17..8]	Dn [7]	Dn [6]	Dn [5]	Dn [4]	Dn [3]	Dn [2]	Dn [1]	Dn [0]	000 3FF
Description	This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write_memory_continue or write_memory_start command. **If set_address_mode B5 = 0:** Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value and the column register equals the EC value, or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored. **If set_address_mode B5 = 1:** Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value and the page register equals the EP value, or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored. Sending any other command can stop frame Write. Frame Memory Access and Interface setting (B3h), WEMODE=0 When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the exceeding data will be ignored. Frame Memory Access and Interface setting (B3h), WEMODE=1 When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the column and page number will be reset, and the exceeding data will be written into the following column and page.												
Restriction	A write_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the write address. Otherwise, data written with write_memory_continue is written to undefined addresses.												

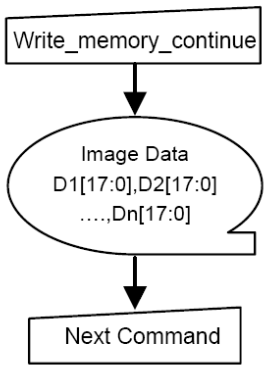
Register Availability

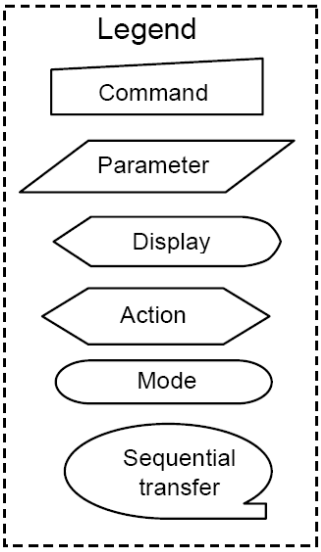
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	No

Default

Status	Default Value
Power On Sequence	Random value
SW Reset	No change
HW Reset	No change

Flow Chart





8.2.35. Read_Memory_Continue (3Eh)

3Eh	Read_Memory_Continue												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	1	1	1	0	3Eh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	D1 [17..8]	D1 [7]	D1 [6]	D1 [5]	D1 [4]	D1 [3]	D1 [2]	D1 [1]	D1 [0]	000 3FF
xst Parameter	1	↑	1	Dx [17..8]	Dx [7]	Dx [6]	Dx [5]	Dx [4]	Dx [3]	Dx [2]	Dx [1]	Dx [0]	000 3FF
Nst Parameter	1	↑	1	Dn [17..8]	Dn [7]	Dn [6]	Dn [5]	Dn [4]	Dn [3]	Dn [2]	Dn [1]	Dn [0]	000 3FF

Description

This command transfers image data from the display module's frame memory to the host processor continuing from the location following the previous read_memory_continue (3Eh) or read_memory_start (2Eh) command.

If set_address_mode B5 = 0:

Pixels are read continuing from the pixel location after the read range of the previous read_memory_start or read_memory_continue. The column register is then incremented and pixels are read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value and the column register equals the EC value, or the host processor sends another command.

If set_address_mode B5 = 1:

Pixels are read continuing from the pixel location after the read range of the previous read_memory_start or read_memory_continue. The page register is then incremented and pixels are read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value and the page register equals the EP value, or the host processor sends another command.

This command makes no change to the other driver status.

Restriction

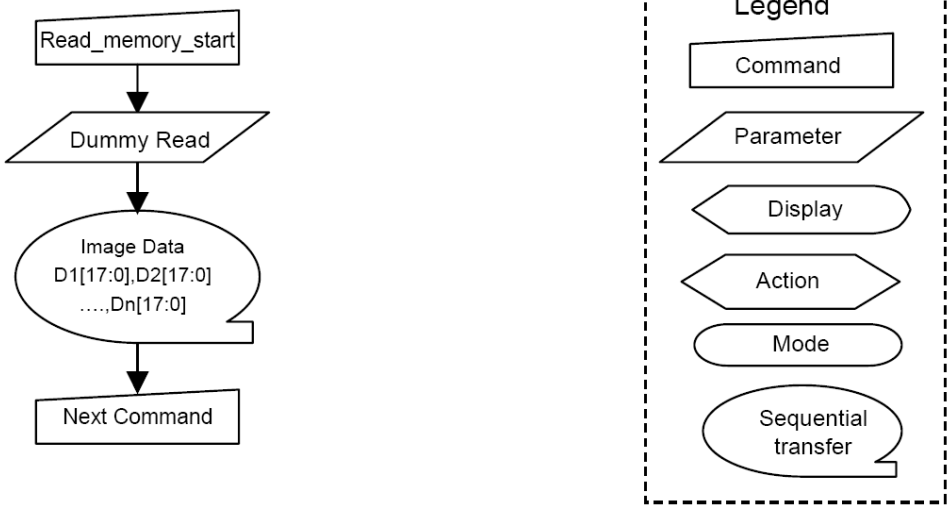
A read_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the read location. Otherwise, data read with read_memory_continue is undefined.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Random data
SW Reset	No change
HW Reset	No change

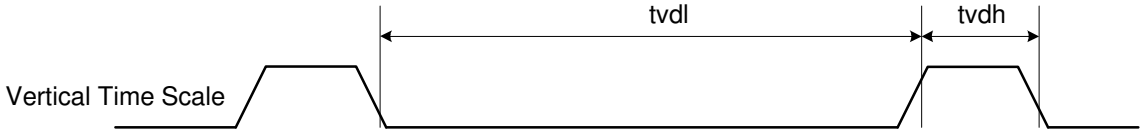
Flow Chart	

8.2.36. Set_Tear_Scanline (44h)

44h	Set_Tear_Scanline												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	0	0	1	0	0	44h
1st Parameter	1	1	↑	XX	0	0	0	0	0	0	0	STS [8]	00
2nd Parameter	1	1	↑	XX	STS [7]	STS [6]	STS [5]	STS [4]	STS [3]	STS [2]	STS [1]	STS [0]	00

Description

This command turns on the display Tearing Effect output signal on the TE signal line when the display reaches line STS. The TE signal is not affected by changing set_address_mode bit B4. The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode.



Note that set_tear_scanline with STS=0 is equivalent to set_tear_on with M=0.

The Tearing Effect Output line shall be active low when the display module is in Sleep mode.

Restriction

-

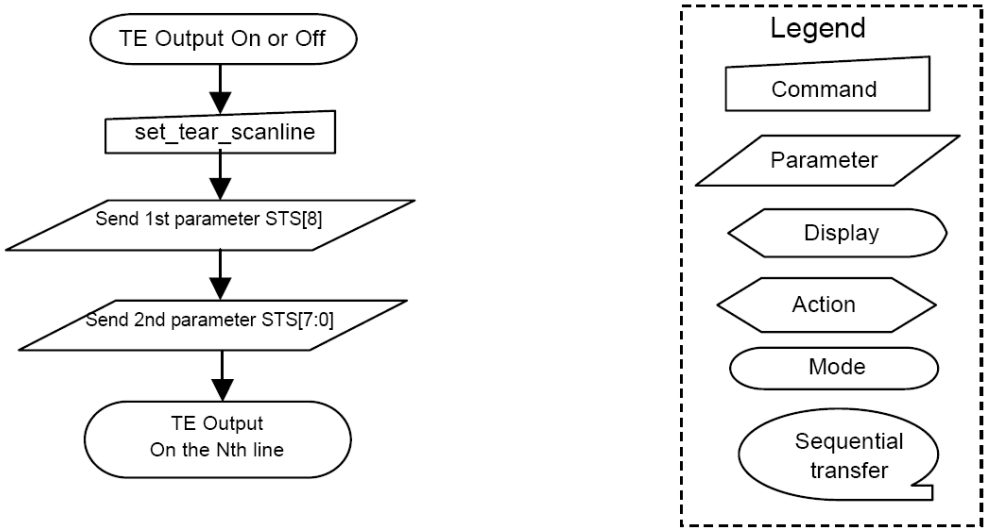
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	STS [8:0]=0000h
SW Reset	STS [8:0]=0000h
HW Reset	STS [8:0]=0000h

Flow Chart



8.2.37. Get_Scanline (45h)

45h	Get_Scanline												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	0	0	1	0	1	45h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	0	0	0	0	0	0	GTS [9]	GTS [8]	00
3rd Parameter	1	↑	1	XX	GTS [7]	GTS [6]	GTS [5]	GTS [4]	GTS [3]	GTS [2]	GTS [1]	GTS [0]	00

Description

The display returns the current scan line, GTS, used to update the display device. The total number of scan lines on a display device is defined as VSYNC + VBP + VACT + VFP. The first scan line is defined as the first line of V-Sync and is denoted as Line 0.

When in Sleep Mode, the value returned by get_scanline is undefined.

Restriction

None

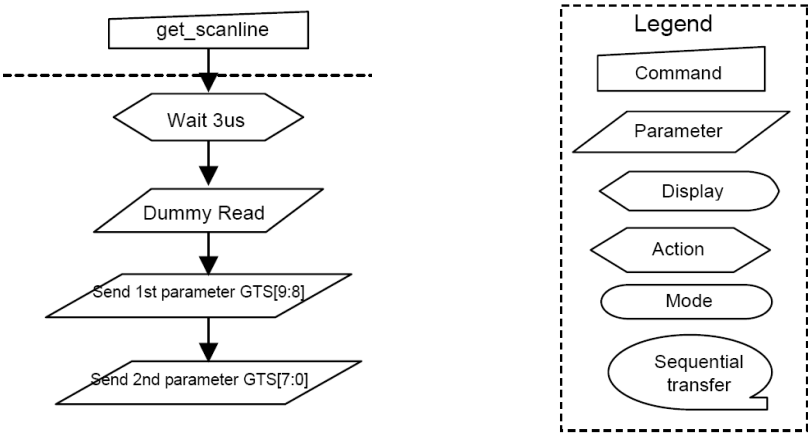
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	GTS [9:0]
Power On Sequence	GTS [9:0]=0000h
SW Reset	GTS [9:0]=0000h
HW Reset	GTS [9:0]=0000h

Flow Chart



8.2.38. Write Display Brightness (51h)

51h	WRDISBV (Write Display Brightness)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	1	0	0	0	1	51h
Parameter	1	1	↑	XX	DBV[7]	DBV[6]	DBV[5]	DBV[4]	DBV[3]	DBV[2]	DBV[1]	DBV[0]	00
Description	This command is used to adjust the brightness value of the display. It should be checked what is the relationship between this written value and output brightness of the display. This relationship is defined on the display module specification. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.												
Restriction	None												

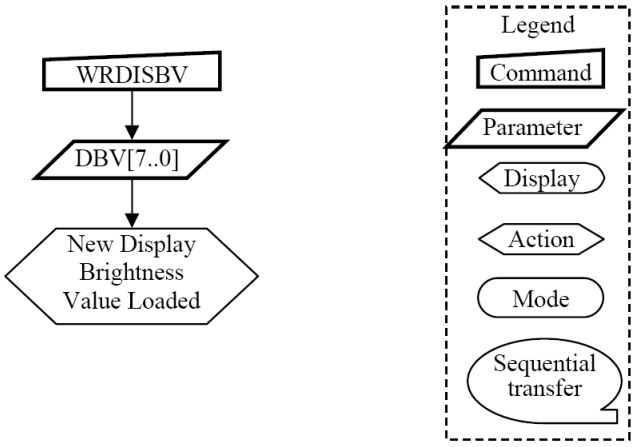
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	DBV [7:0]
Power On Sequence	8'h00h
SW Reset	8'h00h
HW Reset	8'h00h

Flow Chart



8.2.39. Read Display Brightness (52h)

52h	RDDISBV (Read Display Brightness Value)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	1	0	0	1	0	52h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	DBV[7]	DBV[6]	DBV[5]	DBV[4]	DBV[3]	DBV[2]	DBV[1]	DBV[0]	00

Description

This command returns the brightness value of the display.

It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification.

In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.

Restriction

The display module is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on DBI Mode.

Only 2nd parameter is sent on DSI (The 1st parameter is not sent).

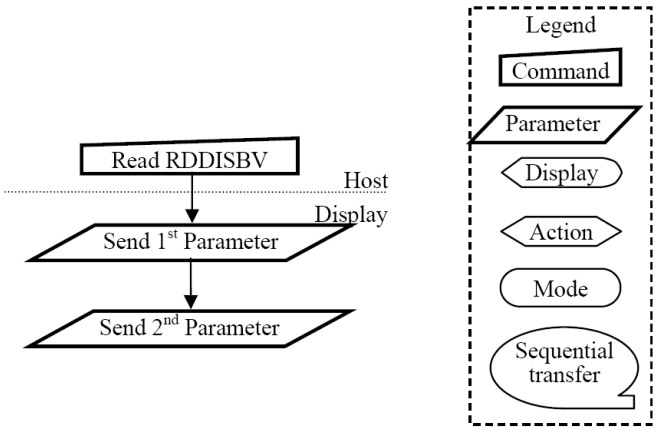
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	DBV [7:0]
Power On Sequence	8'h00h
SW Reset	8'h00h
HW Reset	8'h00h

Flow Chart



8.2.40. Write CTRL Display (53h)

53h	WRCTRLD (Write Control Display)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	1	0	0	1	1	53h
Parameter	1	1	↑	XX	0	0	BCTRL	0	DD	BL	0	0	00

Description

This command is used to control display brightness.

BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display.

0 = Off (Brightness registers are 00h, DBV[7..0])

1 = On (Brightness registers are active, according to the other parameters.)

DD: Display Dimming, only for manual brightness setting

DD = 0: Display Dimming is off

DD = 1: Display Dimming is on

BL: Backlight Control On/Off

0 = Off (Completely turn off backlight circuit. Control lines must be low.)

1 = On

Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 → 1 or 1→ 0.

When BL bit change from “On” to “Off”, backlight is turned off without gradual dimming, even if dimming-on (DD=1) are selected.

Restriction

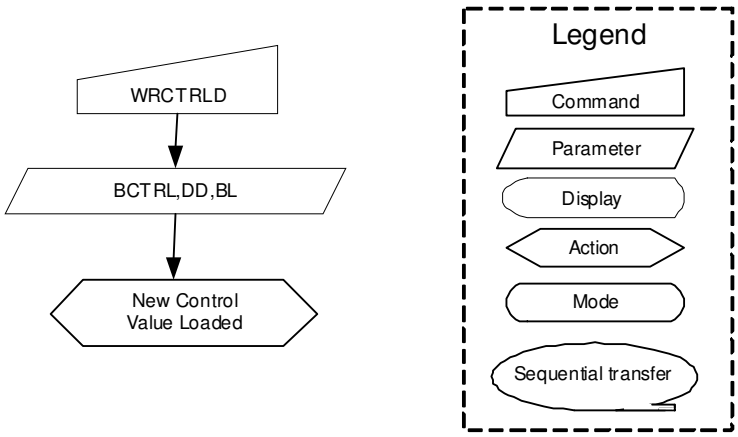
None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	BCTRL	DD	BL
Power On Sequence	1’b0	1’b0	1’b0
SW Reset	1’b0	1’b0	1’b0
HW Reset	1’b0	1’b0	1’b0

Flow Chart	

8.2.41. Read CTRL Display (54h)

54h	RDCTRLD (Read Control Display)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	1	0	1	0	0	54h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XX	0	0	BCTRL	0	DD	BL	0	0	00

Description

This command is used to return brightness setting.

BCTRL: Brightness Control Block On/Off,

'0' = Off (Brightness registers are 00h)

'1' = On (Brightness registers are active, according to the DBV[7..0] parameters.)

DD: Display Dimming

'0' = Display Dimming is off

'1' = Display Dimming is on

BL: Backlight On/Off

'0' = Off (Completely turn off backlight circuit. Control lines must be low.)

'1' = On

Restriction

The display module is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on DBI.

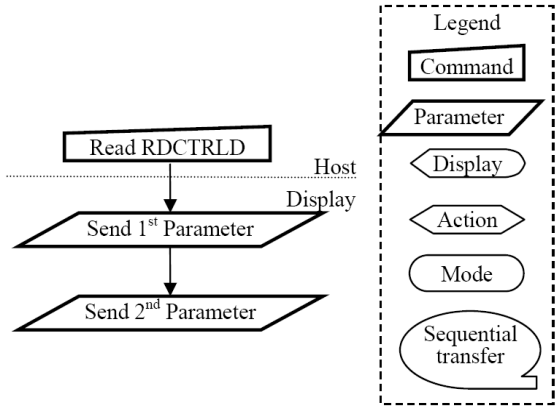
Only 2nd parameter is sent on DSI (The 1st parameter is not sent).

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	BCTRL	DD	BL
Power On Sequence	1'b0	1'b0	1'b0
SW Reset	1'b0	1'b0	1'b0
HW Reset	1'b0	1'b0	1'b0

Flow Chart	

8.2.42. Write Content Adaptive Brightness Control (55h)

55h	WRCABC (Write Content Adaptive Brightness Control)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	1	0	1	0	1	55h
Parameter	1	1	↑	XX	0	0	0	0	0	0	C [1]	C [0]	00

Description

This command is used to set parameters for image content based adaptive brightness control functionality.

There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

C [1:0]	Default Value
2'b00	Off
2'b01	User Interface Image
2'b10	Still Picture
2'b11	Moving Image

Restriction

None

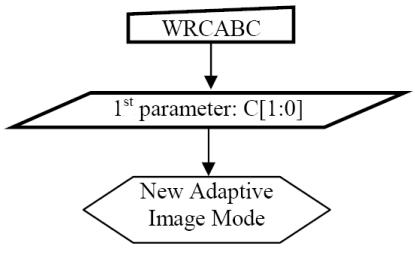
Register Availability

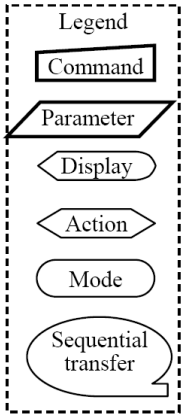
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	C [1:0]=00h
SW Reset	C [1:0]=00h
HW Reset	C [1:0]=00h

Flow Chart





8.2.43. Read Content Adaptive Brightness Control (56h)

56h	RDCABC (Read Content Adaptive Brightness Control)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	1	0	1	1	0	56h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XX	0	0	0	0	0	0	C [1]	C [0]	00

Description

This command is used to read the settings for image content based adaptive brightness control functionality.

It is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

C [1:0]	Default Value
2'b00	Off
2'b01	User Interface Image
2'b10	Still Picture
2'b11	Moving Image

Restriction

The display module is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on DBI.

Only 2nd parameter is sent on DSI (The 1st parameter is not sent).

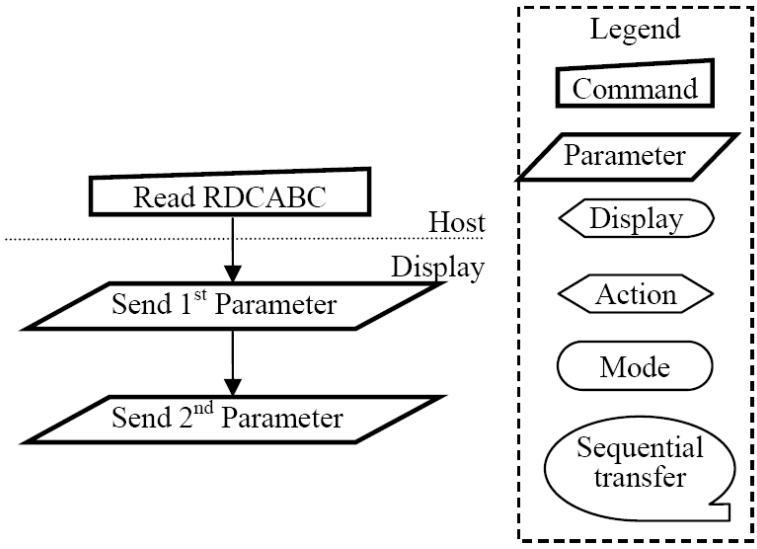
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	C [1:0]=00h
SW Reset	C [1:0]=00h
HW Reset	C [1:0]=00h

Flow Chart



8.2.44. Write CABC Minimum Brightness (5Eh)

5Eh	Backlight Control 1												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	1	1	1	1	0	5Eh
Parameter	1	1	↑	XX	CMB [7]	CMB [6]	CMB [5]	CMB [4]	CMB [3]	CMB [2]	CMB [1]	CMB [0]	00
Description	This command is used to set the minimum brightness value of the display for CABC function. CMB[7:0]: CABC minimum brightness control, this parameter is used to avoid too much brightness reduction. When CABC is active, CABC cannot reduce the display brightness to less than CABC minimum brightness setting. Image processing function is worked as normal, even if the brightness cannot be changed. This function does not affect to the other function, manual brightness setting. Manual brightness can be set the display brightness to less than CABC minimum brightness. Smooth transition and dimming function can be worked as normal. When display brightness is turned off (BCTRL=0 of "Write CTRL Display (53h)"), CABC minimum brightness setting is ignored. In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	CMB [7:0]
Power On Sequence	8'h00h
SW Reset	No Change
HW Reset	8'h00h

8.2.45. Read CABC Minimum Brightness (5Fh)

5Fh	Backlight Control 1												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	1	1	1	1	1	5Fh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	CMB [7]	CMB [6]	CMB [5]	CMB [4]	CMB [3]	CMB [2]	CMB [1]	CMB [0]	00

Description

This command returns the minimum brightness value of CABC function.

In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.

CMB[7:0] is CABC minimum brightness specified with "Write CABC minimum brightness (5Eh)" command. In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	CMB [7:0]
Power On Sequence	8'h00h
SW Reset	No Change
HW Reset	8'h00h

8.2.46. Read ID1 (DAh)

DAh	RDID1 (Read ID1)											
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	1	0	1	0	DAh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	ID1 [7:0]								XX
Description	This read byte identifies the LCD module's manufacturer ID and it is specified by User The 1st parameter is dummy data. The 2nd parameter is LCD module's manufacturer ID. X = Don't care												
Restriction													

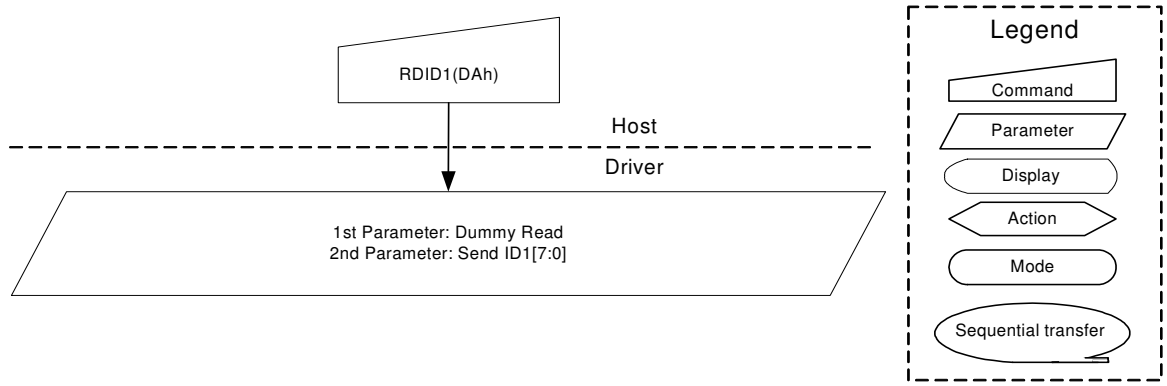
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Before MTP program)	Default Value (After MTP program)
Power On Sequence	8'h00h	MTP value
SW Reset	8'h00h	MTP value
HW Reset	8'h00h	MTP value

Flow Chart



8.2.47. Read ID2 (DBh)

DBh	RDID2 (Read ID2)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	1	0	1	1	DBh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2ndParameter	1	↑	1	XX	1	ID2 [6:0]							XX
Description	This read byte is used to track the LCD module/driver version. It is defined by display supplier (with User's agreement) and changes each time a revision is made to the display, material or construction specifications. The 1st parameter is dummy data. The 2nd parameter is LCD module/driver version ID and the ID parameter range is from 80h to FFh. The ID2 can be programmed by MTP function. X = Don't care												
Restriction													

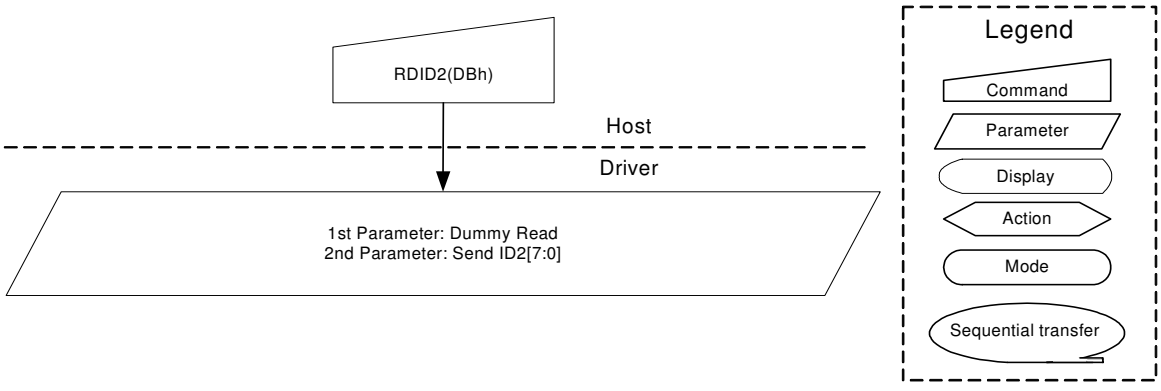
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Before MTP program)	Default Value (After MTP program)
Power On Sequence	8'h80h	MTP value
SW Reset	8'h80h	MTP value
HW Reset	8'h80h	MTP value

Flow Chart



8.2.48. Read ID3 (DCh)

DCh	RDID3 (Read ID3)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	1	1	0	0	DCh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	ID3 [7:0]								XX
Description	This read byte identifies the LCD module/driver and It is specified by User. The 1st parameter is dummy data. The 2nd parameter is LCD module/driver ID. The ID3 can be programmed by MTP function. X = Don't care												
Restriction													

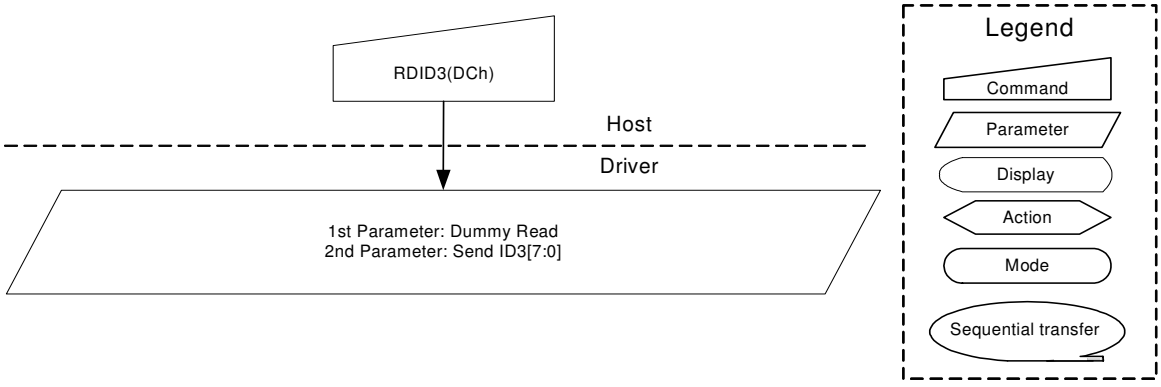
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Before MTP program)	Default Value (After MTP program)
Power On Sequence	8'h00h	MTP value
SW Reset	8'h00h	MTP value
HW Reset	8'h00h	MTP value

Flow Chart



8.3. Description of Level 2 Command

8.3.1. RGB Interface Signal Control (B0h)

<table>
<tr><th>B0h</th><th colspan="12">IFMODE (Interface Mode Control)</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>B0h</td></tr>
<tr><td>Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>ByPass_MODE</td><td>RCM [1]</td><td>RCM [0]</td><td>0</td><td>VSPL</td><td>HSPL</td><td>DPL</td><td>EPL</td><td>40</td></tr>
<tr><td>Description</td><td colspan="13">Sets the operation status of the display interface. The setting becomes effective as soon as the command is received.
EPL: DE polarity (“0”= High enable for RGB interface, “1”= Low enable for RGB interface)
DPL: DOTCLK polarity set (“0”= data fetched at the rising time, “1”= data fetched at the falling time)
HSPL: HSYNC polarity (“0”= Low level sync clock, “1”= High level sync clock)
VSPL: VSYNC polarity (“0”= Low level sync clock, “1”= High level sync clock)
RCM [1:0]: RGB interface selection (refer to the RGB interface section).

ByPass_MODE: Select display data path whether Memory or Direct to Shift register when RGB Interface is used.
<table>
<tr><th>ByPass_MODE</th><th>Display Data Path</th></tr>
<tr><td>0</td><td>Direct to Shift Register (default)</td></tr>
<tr><td>1</td><td>Memory</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13">EXTC should be high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Sleep IN</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th rowspan="2">Status</th><th colspan="6">Default Value</th></tr>
<tr><th>ByPass_MODE</th><th>RCM [1:0]</th><th>VSPL</th><th>HSPL</th><th>DPL</th><th>EPL</th></tr>
<tr><td>Power ON Sequence</td><td>1’b0</td><td>2’b10</td><td>1’b0</td><td>1’b0</td><td>1’b0</td><td>1’b0</td></tr>
<tr><td>SW Reset</td><td>1’b0</td><td>2’b10</td><td>1’b0</td><td>1’b0</td><td>1’b0</td><td>1’b0</td></tr>
<tr><td>HW Reset</td><td>1’b0</td><td>2’b10</td><td>1’b0</td><td>1’b0</td><td>1’b0</td><td>1’b0</td></tr>
</table></td></tr>
</table>

8.3.2. Frame Rate Control (In Normal Mode/Full Colors) (B1h)

B1h	FRMCTR1 (Frame Rate Control (In Normal Mode / Full colors))												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	0	0	1	B1h
1st Parameter	1	1	↑	XX	0	0	0	0	0	0	DIVA [1:0]		00
2nd Parameter	1	1	↑	XX	0	0	0	RTNA [4:0]					1B

Description

Formula to calculate frame frequency:

$$\text{Frame Rate} = \frac{\text{fosc}}{\text{Clocks per line x Division ratio x (Lines + VBP + VFP)}}$$

Sets the division ratio for internal clocks of Normal mode at MCU interface.

fosc : internal oscillator frequency(Oscillator/26)

Clocks per line : RTNA setting

Division ratio : DIVA setting

Lines : total driving line number

VBP : back porch line number

VFP : front porch line number

RTNA [4:0]					Frame Rate (Hz)
1	0	0	0	0	119
1	0	0	0	1	112
1	0	0	1	0	106
1	0	0	1	1	100
1	0	1	0	0	95
1	0	1	0	1	90
1	0	1	1	0	86
1	0	1	1	1	83

RTNA [4:0]					Frame Rate (Hz)
1	1	0	0	0	79
1	1	0	0	1	76
1	1	0	1	0	73
1	1	0	1	1	70(default)
1	1	1	0	0	68
1	1	1	0	1	65
1	1	1	0	1	63
1	1	1	1	1	61

DIVA [1:0] : division ratio for internal clocks when Normal mode.

DIVA [1:0]		Division Ratio
0	0	fosc
0	1	fosc / 2
1	0	fosc / 4
1	1	fosc / 8

RTNA [4:0] : RTNA[4:0] is used to set 1H (line) period of Normal mode at MCU interface.

RTNA [4:0]					Clock per Line
0	0	0	0	0	Setting prohibited
0	0	0	0	1	Setting prohibited
0	0	0	1	0	Setting prohibited
0	0	0	1	1	Setting prohibited
0	0	1	0	0	Setting prohibited
0	0	1	0	1	Setting prohibited
0	0	1	1	0	Setting prohibited
0	0	1	1	1	Setting prohibited
0	1	0	0	0	Setting prohibited
0	1	0	0	1	Setting prohibited
0	1	0	1	0	Setting prohibited

RTNA [4:0]					Clock per Line
0	1	0	1	1	Setting prohibited
0	1	1	0	0	Setting prohibited
0	1	1	0	1	Setting prohibited
0	1	1	1	0	Setting prohibited
0	1	1	1	1	Setting prohibited
1	0	0	0	0	16 clocks
1	0	0	0	1	17 clocks
1	0	0	1	0	18 clocks
1	0	0	1	1	19 clocks
1	0	1	0	0	20 clocks
1	0	1	0	1	21 clocks

RTNA [4:0]					Clock per Line
1	0	1	1	0	22 clocks
1	0	1	1	1	23 clocks
1	1	0	0	0	24 clocks
1	1	0	0	1	25 clocks
1	1	0	1	0	26 clocks
1	1	0	1	1	27 clocks
1	1	1	0	0	28 clocks
1	1	1	0	1	29 clocks
1	1	1	1	0	30 clocks
1	1	1	1	1	31 clocks

<table>
<tr><td>Restriction</td><td>EXTC should be high to enable this command</td></tr>
<tr><td>Register
Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Sleep IN</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr>
<tr><th>DIVA [1:0]</th><th>RTNA [4:0]</th></tr>
<tr><td>Power ON Sequence</td><td>2’b00</td><td>5’h1Bh</td></tr>
<tr><td>SW Reset</td><td>2’b00</td><td>5’h1Bh</td></tr>
<tr><td>HW Reset</td><td>2’b00</td><td>5’h1Bh</td></tr>
</table>
</td></tr>
</table>

8.3.3. Frame Rate Control (In Idle Mode/8 colors) (B2h)

B2h	FRMCTR2 (Frame Rate Control (In Idle Mode / 8l colors))												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	0	1	0	B2h
1st Parameter	1	1	↑	XX	0	0	0	0	0	0	DIVB [1:0]		00
2ndParameter	1	1	↑	XX	0	0	0	RTNB [4:0]					1B

Description

Formula to calculate frame frequency

$$\text{Frame Rate} = \frac{\text{fosc}}{\text{Clocks per line x Division ratio x (Lines + VBP + VFP)}}$$

Sets the division ratio for internal clocks of Idle mode at MCU interface.

fosc : internal oscillator frequency(Oscillator/26)

Clocks per line : RTNB setting

Division ratio : DIVB setting

Lines : total driving line number

VBP : back porch line number

VFP : front porch line number

RTNB [4:0]					Frame Rate (Hz)
1	0	0	0	0	119
1	0	0	0	1	112
1	0	0	1	0	106
1	0	0	1	1	100
1	0	1	0	0	95
1	0	1	0	1	90
1	0	1	1	0	86
1	0	1	1	1	83

RTNB [4:0]					Frame Rate (Hz)
1	1	0	0	0	79
1	1	0	0	1	76
1	1	0	1	0	73
1	1	0	1	1	70(default)
1	1	1	0	0	68
1	1	1	0	1	65
1	1	1	0	1	63
1	1	1	1	1	61

DIVB [1:0]: division ratio for internal clocks when Idle mode.

DIVB [1:0]		Division Ratio
0	0	fosc
0	1	fosc / 2
1	0	fosc / 4
1	1	fosc / 8

RTNB [4:0]: RTNB[4:0] is used to set 1H (line) period of Idle mode at MCU interface.

RTNB [4:0]					Clock per Line
0	0	0	0	0	Setting prohibited
0	0	0	0	1	Setting prohibited
0	0	0	1	0	Setting prohibited
0	0	0	1	1	Setting prohibited
0	0	1	0	0	Setting prohibited
0	0	1	0	1	Setting prohibited
0	0	1	1	0	Setting prohibited
0	0	1	1	1	Setting prohibited
0	1	0	0	0	Setting prohibited
0	1	0	0	1	Setting prohibited
0	1	0	1	0	Setting prohibited

RTNB [4:0]					Clock per Line
0	1	0	1	1	Setting prohibited
0	1	1	0	0	Setting prohibited
0	1	1	0	1	Setting prohibited
0	1	1	1	0	Setting prohibited
0	1	1	1	1	Setting prohibited
1	0	0	0	0	16 clocks
1	0	0	0	1	17 clocks
1	0	0	1	0	18 clocks
1	0	0	1	1	19 clocks
1	0	1	0	0	20 clocks
1	0	1	0	1	21 clocks

RTNB [4:0]					Clock per Line
1	0	1	1	0	22 clocks
1	0	1	1	1	23 clocks
1	1	0	0	0	24 clocks
1	1	0	0	1	25 clocks
1	1	0	1	0	26 clocks
1	1	0	1	1	27 clocks
1	1	1	0	0	28 clocks
1	1	1	0	1	29 clocks
1	1	1	1	0	30 clocks
1	1	1	1	1	31 clocks

<table>
<tr><td>Restriction</td><td>EXTC should be high to enable this command</td></tr>
<tr><td>Register
Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Sleep IN</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr>
<tr><th>DIVB [1:0]</th><th>RTNB [4:0]</th></tr>
<tr><td>Power ON Sequence</td><td>2’b00</td><td>5’h1Bh</td></tr>
<tr><td>SW Reset</td><td>2’b00</td><td>5’h1Bh</td></tr>
<tr><td>HW Reset</td><td>2’b00</td><td>5’h1Bh</td></tr>
</table>
</td></tr>
</table>

8.3.4. Frame Rate control (In Partial Mode/Full Colors) (B3h)

B3h	FRMCTR3 (Frame Rate Control (In Partial Mode / Full colors))												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	0	1	1	B3h
1st Parameter	1	1	↑	XX	0	0	0	0	0	0	DIVC [1:0]		00
2ndParameter	1	1	↑	XX	0	0	0	RTNC [4:0]					1B

Description

Formula to calculate frame frequency:

$$\text{Frame Rate} = \frac{\text{fosc}}{\text{Clocks per line x Division ratio x (Lines + VBP + VFP)}}$$

Sets the division ratio for internal clocks of Partial mode (Idle mode off) at MCU interface.

fosc : internal oscillator frequency(Oscillator/26)

Clocks per line : RTNC setting

Division ratio : DIVC setting

Lines : total driving line number

VBP : back porch line number

VFP : front porch line number

RTNC [4:0]					Frame Rate (Hz)
1	0	0	0	0	119
1	0	0	0	1	112
1	0	0	1	0	106
1	0	0	1	1	100
1	0	1	0	0	95
1	0	1	0	1	90
1	0	1	1	0	86
1	0	1	1	1	83

RTNC [4:0]					Frame Rate (Hz)
1	1	0	0	0	79
1	1	0	0	1	76
1	1	0	1	0	73
1	1	0	1	1	70(default)
1	1	1	0	0	68
1	1	1	0	1	65
1	1	1	0	1	63
1	1	1	1	1	61

DIVC [1:0]: division ratio for internal clocks when Partial mode.

DIVC [1:0]		Division Ratio
0	0	fosc
0	1	fosc / 2
1	0	fosc / 4
1	1	fosc / 8

RTNC [4:0]: RTNC [4:0] is used to set 1H (line) period of Partial mode at MCU interface.

RTNC [4:0]					Clock per Line
0	0	0	0	0	Setting prohibited
0	0	0	0	1	Setting prohibited
0	0	0	1	0	Setting prohibited
0	0	0	1	1	Setting prohibited
0	0	1	0	0	Setting prohibited
0	0	1	0	1	Setting prohibited
0	0	1	1	0	Setting prohibited
0	0	1	1	1	Setting prohibited
0	1	0	0	0	Setting prohibited
0	1	0	0	1	Setting prohibited
0	1	0	1	0	Setting prohibited

RTNC [4:0]					Clock per Line
0	1	0	1	1	Setting prohibited
0	1	1	0	0	Setting prohibited
0	1	1	0	1	Setting prohibited
0	1	1	1	0	Setting prohibited
0	1	1	1	1	Setting prohibited
1	0	0	0	0	16 clocks
1	0	0	0	1	17 clocks
1	0	0	1	0	18 clocks
1	0	0	1	1	19 clocks
1	0	1	0	0	20 clocks
1	0	1	0	1	21 clocks

RTNC [4:0]					Clock per Line
1	0	1	1	0	22 clocks
1	0	1	1	1	23 clocks
1	1	0	0	0	24 clocks
1	1	0	0	1	25 clocks
1	1	0	1	0	26 clocks
1	1	0	1	1	27 clocks
1	1	1	0	0	28 clocks
1	1	1	0	1	29 clocks
1	1	1	1	0	30 clocks
1	1	1	1	1	31 clocks

<table>
<tr><td>Restriction</td><td>EXTC should be high to enable this command</td></tr>
<tr><td>Register
Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Sleep IN</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr>
<tr><th>DIVC [1:0]</th><th>RTNC [4:0]</th></tr>
<tr><td>Power ON Sequence</td><td>2’b00</td><td>5’h1Bh</td></tr>
<tr><td>SW Reset</td><td>2’b00</td><td>5’h1Bh</td></tr>
<tr><td>HW Reset</td><td>2’b00</td><td>5’h1Bh</td></tr>
</table>
</td></tr>
</table>

8.3.5. Display Inversion Control (B4h)

B4h	INVTR (Display Inversion Control)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	1	0	0	B4h
1st Parameter	1	1	↑	XX	0	0	0	0	0	NLA	NLB	NLC	02
2ndParameter	1	1	↑	XX	0	0	NW [5:0]						00

Description

Display inversion mode set

NLA: Inversion setting in full colors normal mode (Normal mode on)

NLB: Inversion setting in Idle mode (Idle mode on)

NLC: Inversion setting in full colors partial mode (Partial mode on / Idle mode off)

NLA / NLB / NLC	Inversion
0	Line inversion
1	Frame inversion

NW [5:0]: N-line inversion setting in NLA=0, NLB=0 and NLC=0.

NW [5:0]						N-line Inversion
0	0	0	0	0	0	1 lines
0	0	0	0	0	1	2 lines
0	0	0	0	1	0	3 lines
0	0	0	0	1	1	4 lines
0	0	0	1	0	0	5 lines
0	0	0	1	0	1	6 lines
0	0	0	1	1	0	7 lines
0	0	0	1	1	1	8 lines
0	0	1	0	0	0	9 lines
0	0	1	0	0	1	10 lines
0	0	1	0	1	0	11 lines
0	0	1	0	1	1	12 lines
0	0	1	1	0	0	13 lines
0	0	1	1	0	1	14 lines
0	0	1	1	1	0	15 lines
0	0	1	1	1	1	16 lines
0	1	0	0	0	0	17 lines
0	1	0	0	0	1	18 lines
0	1	0	0	1	0	19 lines
0	1	0	0	1	1	20 lines
0	1	0	1	0	0	21 lines
0	1	0	1	0	1	22 lines
0	1	0	1	1	0	23 lines
0	1	0	1	1	1	24 lines
0	1	1	0	0	0	25 lines
0	1	1	0	0	1	26 lines
0	1	1	0	1	0	27 lines
0	1	1	0	1	1	28 lines
0	1	1	1	0	0	29 lines
0	1	1	1	0	1	30 lines
0	1	1	1	1	0	31 lines
0	1	1	1	1	1	32 lines

NW [5:0]						N-line Inversion
1	0	0	0	0	0	33 lines
1	0	0	0	0	1	34 lines
1	0	0	0	1	0	35 lines
1	0	0	0	1	1	36 lines
1	0	0	1	0	0	37 lines
1	0	0	1	0	1	38 lines
1	0	0	1	1	0	39 lines
1	0	0	1	1	1	40 lines
1	0	1	0	0	0	41 lines
1	0	1	0	0	1	42 lines
1	0	1	0	1	0	43 lines
1	0	1	0	1	1	44 lines
1	0	1	1	0	0	45 lines
1	0	1	1	0	1	46 lines
1	0	1	1	1	0	47 lines
1	0	1	1	1	1	48 lines
1	1	0	0	0	0	49 lines
1	1	0	0	0	1	50 lines
1	1	0	0	1	0	51 lines
1	1	0	0	1	1	52 lines
1	1	0	1	0	0	53 lines
1	1	0	1	0	1	54 lines
1	1	0	1	1	0	55 lines
1	1	0	1	1	1	56 lines
1	1	1	0	0	0	57 lines
1	1	1	0	0	1	58 lines
1	1	1	0	1	0	59 lines
1	1	1	0	1	1	60 lines
1	1	1	1	0	0	61 lines
1	1	1	1	0	1	62 lines
1	1	1	1	1	0	63 lines
1	1	1	1	1	1	64 lines

Restriction	EXTC should be high to enable this command

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value			
	NLA	NLB	NLC	NW [5:0]
Power ON Sequence	1'b0	1'b1	1'b0	6'h00h
SW Reset	1'b0	1'b1	1'b0	6'h00h
H/W Reset	1'b0	1'b1	1'b0	6'h00h

8.3.6. Blanking Porch Control (B5h)

B5h	PRCTR (Blanking Porch)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	1	0	1	B5h
1st Parameter	1	1	↑	XX	0	VFP [6:0]							02
2nd Parameter	1	1	↑	XX	0	VBP [6:0]							02
3rd Parameter	1	1	↑	XX	0	0	0	HFP [4:0]					0A
4th Parameter	1	1	↑	XX	0	0	0	HBP [4:0]					14

Description

VFP [6:0] / **VBP [6:0]:** The VFP [6:0] and VBP [6:0] bits specify the line number of vertical front and back porch period respectively.

VFP [6:0] VBP [6:0]	Number of HSYNC of front/back porch	VFP [6:0] VBP [6:0]	Number of HSYNC of front/back porch
0000000	Setting inhibited	1000000	64
0000001	Setting inhibited	1000001	65
0000010	2	1000010	66
0000011	3	1000011	67
0000100	4	1000100	68
0000101	5	1000101	69
0000110	6	1000110	70
0000111	7	1000111	71
0001000	8	1001000	72
0001001	9	1001001	73
0001010	10	1001010	74
0001011	11	1001011	75
0001100	12	1001100	76
0001101	13	1001101	77
: :	: :	: :	: :
0111101	61	1111101	125
0111110	62	1111110	126
0111111	63	1111111	127

Note: VFP + VBP ≦ 254 HSYNC signals

HFP [4:0] / **HBP [4:0]:** The HFP [4:0] and HBP [4:0] bits specify the line number of horizontal front and back porch period respectively.

HFP [4:0] HBP [4:0]	Number of DOTCLK of the front/back porch	HFP [4:0] HBP [4:0]	Number of DOTCLK of front/back porch
00000	Setting prohibited	10000	16
00001	Setting prohibited	10001	17
00010	2	10010	18
00011	3	10011	19
00100	4	10100	20
00101	5	10101	21
00110	6	10110	22
00111	7	10111	23
01000	8	11000	24
01001	9	11001	25
01010	10	11010	26
01011	11	11011	27
01100	12	11100	28
01101	13	11101	29
01110	14	11110	30
01111	15	11111	31

**HBP need to setting more than 58 clock and less than 200 clocks in By-pass mode. There is 8 bit setting in HBP register.*

<table>
<tr><td>Restriction</td><td>EXTC should be high to enable this command</td></tr>
<tr><td>Register
Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Sleep IN</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="4">Default Value</th></tr>
<tr><th>VFP [6:0]</th><th>VBP [6:0]</th><th>HFP [4:0]</th><th>HBP [4:0]</th></tr>
<tr><td>Power ON Sequence</td><td>7’h02h</td><td>7’h02h</td><td>5’h0Ah</td><td>5’h14h</td></tr>
<tr><td>SW Reset</td><td>7’h02h</td><td>7’h02h</td><td>5’h0Ah</td><td>5’h14h</td></tr>
<tr><td>HW Reset</td><td>7’h02h</td><td>7’h02h</td><td>5’h0Ah</td><td>5’h14h</td></tr>
</table>
</td></tr>
</table>

8.3.7. Display Function Control (B6h)

B6h	DISCTRL (Display Function Control)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	1	1	0	B6h
1st Parameter	1	1	↑	XX	0	0	0	0	PTG [1:0]		PT [1:0]		0A
2nd Parameter	1	1	↑	XX	REV	GS	SS	SM	ISC [3:0]				82
3rd Parameter	1	1	↑	XX	0	0	NL [5:0]						27
4th Parameter	1	1	↑	XX	0	0	PCDIV [5:0]						XX

Description

PTG [1:0]: Set the scan mode in non-display area.

PTG1	PTG0	Gate outputs in non-display area	Source outputs in non-display area	VCOM output
0	0	Normal scan	Set with the PT [2:0] bits	VCOMH/VCOML
0	1	Setting prohibited	---	---
1	0	Interval scan	Set with the PT [2:0] bits	
1	1	Setting prohibited	---	---

PT [1:0]: Determine source/VCOM output in a non-display area in the partial display mode.

PT [1:0]		Source output on non-display area		VCOM output on non-display area	
		Positive polarity	Negative polarity	Positive polarity	Negative polarity
0	0	V63	V0	VCOML	VCOMH
0	1	V0	V63	VCOML	VCOMH
1	0	AGND	AGND	AGND	AGND
1	1	Hi-Z	Hi-Z	AGND	AGND

SS: This bit controls MPU to memory write/read direction by column address order.

REV: Select whether the liquid crystal type is normally white type or normally black type.

REV	Liquid crystal type
0	Normally black
1	Normally white

ISC [3:0]: Specify the scan cycle interval of gate driver in non-display area when PTG [1:0] ="10" to select interval scan.

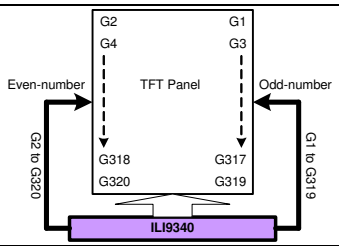
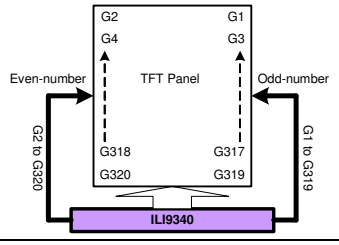
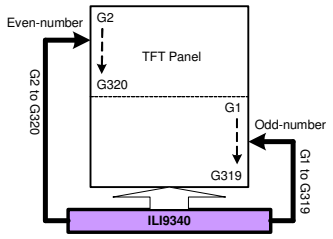
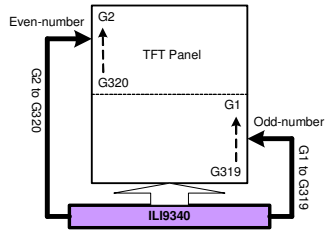
Then scan cycle is set as odd number from 0~29 frame periods. The polarity is inverted every scan cycle.

ISC [3:0]	Scan Cycle	f_{FLM} = 60Hz
0000	1 frame	17ms
0001	3 frames	51ms
0010	5 frames	85ms
0011	7 frames	119ms
0100	9 frames	153ms
0101	11 frames	187ms
0110	13 frames	221ms
0111	15 frames	255ms
1000	17 frames	289ms
1001	19 frames	323ms
1010	21 frames	357ms
1011	23 frames	391ms
1100	25 frames	425ms
1101	27 frames	459ms
1110	29 frames	493ms
1111	31 frames	527ms

GS: Sets the direction of scan by the gate driver in the range determined by SCN [4:0] and NL [4:0]. The scan direction determined by GS = 0 can be reversed by setting GS = 1.

GS	Gate Output Scan Direction
0	G1 → G320
1	G320 → G1

SM: Sets the gate driver pin arrangement in combination with the GS bit to select the optimal scan mode for the module.

SM	GS	Scan Direction	Gate Output Sequence
0	0		G1→G2→G3→G4→ …… ….→G317→G318→G319→G320
0	1		G320→G319->G318→G317→…… …. →G4→G3→G2→G1
1	0		G1→G3→…….....→G317→G319→ G2→G4→……→G318→G320
1	1		G320, G318, G316, …, G10, G8, G6, G4, G2 G319, G317, G315, …, G9, G78, G5, G3, G1 G320→G318→…….....→G4→G2→ G319→G317→……→G3→G1

NL [5:0]: Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL [5:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

NL [5:0]						LCD Drive Line
0	0	0	0	0	0	Setting prohibited
0	0	0	0	0	1	16 lines
0	0	0	0	1	0	24 lines
0	0	0	0	1	1	32 lines
0	0	0	1	0	0	40 lines
0	0	0	1	0	1	48 lines

NL [5:0]						LCD Driver Line
0	1	0	1	0	1	176 lines
0	1	0	1	1	0	184 lines
0	1	0	1	1	1	192 lines
0	1	1	0	0	0	200 lines
0	1	1	0	0	1	208 lines
0	1	1	0	1	0	216 lines

0	0	0	1	1	0	56 lines	0	1	1	0	1	1	224 lines
0	0	0	1	1	1	64 lines	0	1	1	1	0	0	232 lines
0	0	1	0	0	0	72 lines	0	1	1	1	0	1	240 lines
0	0	1	0	0	1	80 lines	0	1	1	1	1	0	248 lines
0	0	1	0	1	0	88 lines	0	1	1	1	1	1	256 lines
0	0	1	0	1	1	96 lines	1	0	0	0	0	0	264 lines
0	0	1	1	0	0	104 lines	1	0	0	0	0	1	272 lines
0	0	1	1	0	1	112 lines	1	0	0	0	1	0	280 lines
0	0	1	1	1	0	120 lines	1	0	0	0	1	1	288 lines
0	0	1	1	1	1	128 lines	1	0	0	1	0	0	296 lines
0	1	0	0	0	0	136 lines	1	0	0	1	0	1	304 lines
0	1	0	0	0	1	144 lines	1	0	0	1	1	0	312 lines
0	1	0	0	1	0	152 lines	1	0	0	1	1	1	320 lines
0	1	0	0	1	1	160 lines	Others						Setting inhibited
0	1	0	1	0	0	168 lines							

PCDIV [5:0]:

$$\text{external fosc} = \frac{\text{DOTCLK}}{2 \times (\text{PCDIV} + 1)}$$

Restriction

EXTC should be high to enable this command

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value							
	PTG [1:0]	PT [1:0]	REV	GS	SS	SM	ISC [3:0]	NL [5:0]
Power ON Sequence	2'b10	2'b10	1'b1	1'b0	1'b0	1'b0	4'b0010	6'h27h
SW Reset	2'b10	2'b10	1'b1	1'b0	1'b0	1'b0	4'b0010	6'h27h
HW Reset	2'b10	2'b10	1'b1	1'b0	1'b0	1'b0	4'b0010	6'h27h

8.3.8. Entry Mode Set (B7h)

B7h	ETMOD (Entry Mode Set)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	1	1	1	B7h
Parameter	1	1	↑	XX	0	0	0	0	0	GON	DTE	GAS	07

Description

GAS: Low voltage detection control.

GAS	Low voltage detection
0	Enable
1	Disable

GON/DTE: Set the output level of gate driver G1 ~ G320 as follows

GON	DTE	G1~G320 Gate Output
0	0	VGH
0	1	VGH
1	0	VGL
1	1	Normal display

Restriction: EXTC should be high to enable this command

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value		
	GON	DTE	GAS
Power ON Sequence	1'b1	1'b1	1'b1
SW Reset	1'b1	1'b1	1'b1
HW Reset	1'b1	1'b1	1'b1

8.3.9. Backlight Control 1 (B8h)

B8h	Backlight Control 1												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	1	0	0	0	B8h
Parameter		1	↑	XX	0	0	0	0	TH_UI [3]	TH_UI [2]	TH_UI [1]	TH_UI [0]	04

Description

TH_UI [3:0]: These bits are used to set the percentage of grayscale data accumulate histogram value in the user interface (UI) mode. This ratio of maximum number of pixels that makes display image white (=data "255") to the total of pixels by image processing.

TH_UI [3:0]	Description
4'0h	99%
4'1h	98%
4'2h	96%
4'3h	94%
4'4h	92%
4'5h	90%
4'6h	88%
4'7h	86%

TH_UI [3:0]	Description
4'8h	84%
4'9h	82%
4'Ah	80%
4'Bh	78%
4'Ch	76%
4'Dh	74%
4'Eh	72%
4'Fh	70%

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	TH_UI [3:0]
Power On Sequence	4'b0100
SW Reset	No change
HW Reset	4'b0100

8.3.10. Backlight Control 2 (B9h)

B9h	Backlight Control 2												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	1	0	0	1	B9h
Parameter	1	1	↑	XX	TH_MV [3]	TH_MV [2]	TH_MV [1]	TH_MV [0]	TH_ST [3]	TH_ST [2]	TH_ST [1]	TH_ST [0]	B8

Description

TH_ST [3:0]: These bits are used to set the percentage of grayscale data accumulate histogram value in the still picture mode. This ratio of maximum number of pixels that makes display image white (=data “255”) to the total of pixels by image processing.

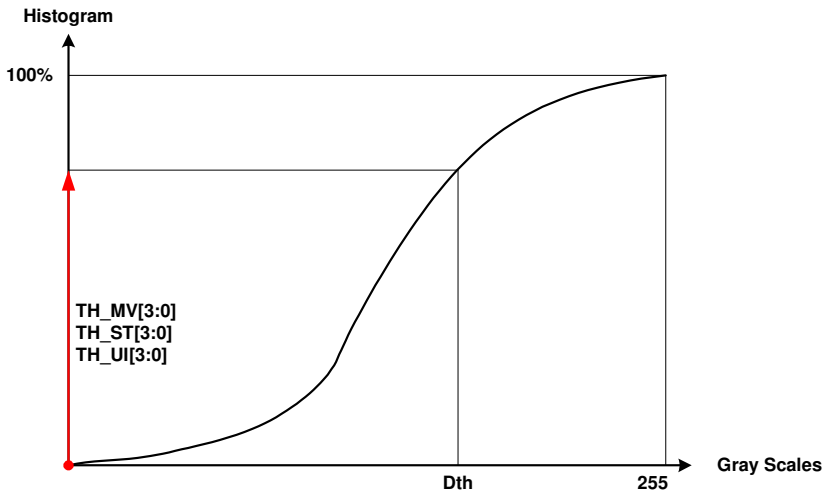
TH_ST [3:0]	Description
4’0h	99%
4’1h	98%
4’2h	96%
4’3h	94%
4’4h	92%
4’5h	90%
4’6h	88%
4’7h	86%

TH_ST [3:0]	Description
4’8h	84%
4’9h	82%
4’Ah	80%
4’Bh	78%
4’Ch	76%
4’Dh	74%
4’Eh	72%
4’Fh	70%

TH_MV [3:0]: These bits are used to set the percentage of grayscale data accumulate histogram value in the moving image mode. This ratio of maximum number of pixels that makes display image white (=data “255”) to the total of pixels by image processing.

TH_MV [3:0]	Description
4’0h	99%
4’1h	98%
4’2h	96%
4’3h	94%
4’4h	92%
4’5h	90%
4’6h	88%
4’7h	86%

TH_MV [3:0]	Description
4’8h	84%
4’9h	82%
4’Ah	80%
4’Bh	78%
4’Ch	76%
4’Dh	74%
4’Eh	72%
4’Fh	70%



Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	TH_MV [3:0]	TH_ST [3:0]
Power On Sequence	4'b1011	4'b1000
SW Reset	No change	No change
HW Reset	4'b1011	4'b1000

8.3.11. Backlight Control 3 (BAh)

BAh	Backlight Control 3												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	1	0	1	0	BAh
Parameter	1	1	↑	XX	0	0	0	0	DTH_UI [3]	DTH_UI [2]	DTH_UI [1]	DTH_UI [0]	04

Description

DTH_UI [3:0]: This parameter is used set the minimum limitation of grayscale threshold value in User Icon (UI) image mode. This register setting will limit the minimum Dth value to prevent the display image from being too white and the display quality is not acceptable.

DTH_UI [3:0]	Description
4'0h	252
4'1h	248
4'2h	244
4'3h	240
4'4h	236
4'5h	232
4'6h	228
4'7h	224

DTH_UI [3:0]	Description
4'8h	220
4'9h	216
4'Ah	212
4'Bh	208
4'Ch	204
4'Dh	200
4'Eh	196
4'Fh	192

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	DTH_UI [3:0]
Power On Sequence	4'b0100
SW Reset	No change
HW Reset	4'b0100

8.3.12. Backlight Control 4 (BBh)

BBh	Backlight Control 4												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	1	0	1	1	BBh
Parameter	1	1	↑	XX	DTH_MV [3]	DTH_MV [2]	DTH_MV [1]	DTH_MV [0]	DTH_ST [3]	DTH_ST [2]	DTH_ST [1]	DTH_ST [0]	C9

Description

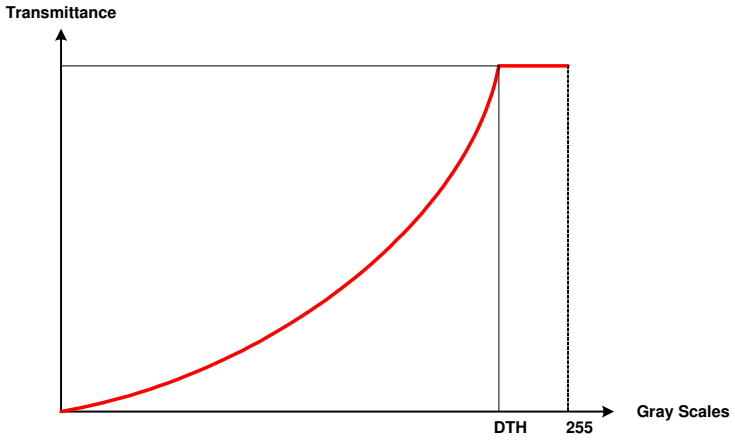
DTH_ST [3:0]/DTH_MV [3:0]: This parameter is used set the minimum limitation of grayscale threshold value. This register setting will limit the minimum Dth value to prevent the display image from being too white and the display quality is not acceptable.

DTH_ST [3:0]	Description
4'0h	224
4'1h	220
4'2h	216
4'3h	212
4'4h	208
4'5h	204
4'6h	200
4'7h	196

DTH_ST [3:0]	Description
4'8h	192
4'9h	188
4'Ah	184
4'Bh	180
4'Ch	176
4'Dh	172
4'Eh	168
4'Fh	164

DTH_MV [3:0]	Description
4'0h	224
4'1h	220
4'2h	216
4'3h	212
4'4h	208
4'5h	204
4'6h	200
4'7h	196

DTH_MV [3:0]	Description
4'8h	192
4'9h	188
4'Ah	184
4'Bh	180
4'Ch	176
4'Dh	172
4'Eh	168
4'Fh	164



Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	DTH_MV [3:0]	DTH_ST [3:0]
Power On Sequence	4'b1100	4'b1001
SW Reset	No change	No change
HW Reset	4'b1100	4'b1001

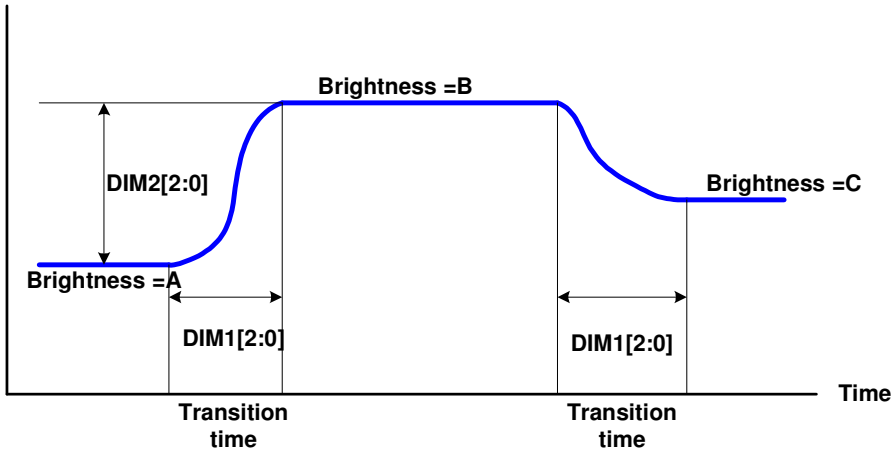
8.3.13. Backlight Control 5 (BCh)

BCh	Backlight Control 5												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	1	1	0	0	BCh
Parameter	1	1	↑	XX	DIM2 [3]	DIM2 [2]	DIM2 [1]	DIM2 [0]	0	DIM1 [2]	DIM1 [1]	DIM1 [0]	44

Description

DIM1 [2:0]: This parameter is used to set the transition time of brightness level to avoid the sharp brightness transition on vision.

DIM1 [2:0]	Description
3'0h	1 frame
3'1h	1 frame
3'2h	2 frames
3'3h	4 frames
3'4h	8 frames
3'5h	16 frames
3'6h	32 frames
3'7h	64 frames



DIM2 [3:0]: This parameter is used to set the threshold of brightness change.

When the brightness transition difference is smaller than DIM2 [3:0], the brightness transition will be ignored.

For example:

If | brightness B – brightness A| < DIM2 [2:0], the brightness transition will be ignored and keep the brightness A.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	DIM2 [3:0]	DIM1 [2:0]
Power On Sequence	4'b0100	4'b0100
SW Reset	No change	No change
HW Reset	4'b0100	4'b0100

8.3.14. Backlight Control 7 (BEh)

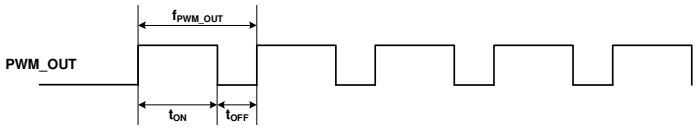
BEh	Backlight Control 7												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	1	1	1	0	BEh
Parameter	1	1	↑	XX	PWM_ DIV[7]	PWM_ DIV[6]	PWM_ DIV[5]	PWM_ DIV[4]	PWM_ DIV[3]	PWM_ DIV[2]	PWM_ DIV[1]	PWM_ DIV[0]	0F

Description

PWM_DIV [7:0]: PWM_OUT output frequency control. This command is used to adjust the PWM waveform frequency of PWM_OUT. The PWM frequency can be calculated by using the following equation.

$$f_{PWM\_OUT} = \frac{16MHz}{(PWM\_DIV[7:0]+1)\times 255}$$

PWM_DIV [7:0]	f_{PWM_OUT}
8'h0	62.74 KHz
8'h1	31.38 KHz
8'h2	20.915KHz
8'h3	15.686KHz
8'h4	12.549 KHz
…	…
8'hFB	249Hz
8'hFC	248Hz
8'hFD	247Hz
8'hFE	246Hz
8'hFF	245Hz



Note: The output frequency tolerance of internal frequency divider in CABC is ±10%

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	PWM_DIV [7:0]=0Fh
SW Reset	No change
HW Reset	PWM_DIV [7:0]=0Fh

8.3.15. Backlight Control 8 (BFh)

BFh	Backlight Control 2												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	1	1	1	1	BFh
Parameter	1	1	↑	XX	0	0	0	0	0	LEDONR	LEDONPOL	LEDPWMPOL	00

Description

LEDPWMPOL: The bit is used to define polarity of LEDPWM signal.

BL	LEDPWMPOL	LEDPWM pin
0	0	0
0	1	1
1	0	Original polarity of PWM signal
1	1	Inversed polarity of PWM signal

LEDONPOL: This bit is used to control LEDON pin.

BL	LEDONPOL	LEDON pin
0	0	0
0	1	1
1	0	LEDONR
1	1	Inversed LEDONR

LEDONR: This bit is used to control LEDON pin.

LEDONR	Description
0	Low
1	High

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	LEDONR	LEDONPOL	LEDPWMPOL
Power On Sequence	1'b0	1'b0	1'b0
SW Reset	No change	No change	No change
HW Reset	1'b0	1'b0	1'b0

8.3.16. Power Control 1 (C0h)

C0h	PWCTRL 1 (Power Control 1)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	0	0	0	0	C0h
1st Parameter	1	1	↑	XX	0	0	VRH [5:0]						26
2nd Parameter	1	1	↑	XX	0	0	0	0	VC [3:0]				00

Description

VRH [5:0]: Set the GVDD level, which is a reference level for the VCOM level and the grayscale voltage level.

VRH [5:0]						GVDD
0	0	0	0	0	0	Setting prohibited
0	0	0	0	0	1	Setting prohibited
0	0	0	0	1	0	Setting prohibited
0	0	0	0	1	1	3.00 V
0	0	0	1	0	0	3.05 V
0	0	0	1	0	1	3.10 V
0	0	0	1	1	0	3.15 V
0	0	0	1	1	1	3.20 V
0	0	1	0	0	0	3.25 V
0	0	1	0	0	1	3.30 V
0	0	1	0	1	0	3.35 V
0	0	1	0	1	1	3.40 V
0	0	1	1	0	0	3.45 V
0	0	1	1	0	1	3.50 V
0	0	1	1	1	0	3.55 V
0	0	1	1	1	1	3.60 V
0	1	0	0	0	0	3.65 V
0	1	0	0	0	1	3.70 V
0	1	0	0	1	0	3.75 V
0	1	0	0	1	1	3.80 V
0	1	0	1	0	0	3.85 V
0	1	0	1	0	1	3.90 V
0	1	0	1	1	0	3.95 V
0	1	0	1	1	1	4.00 V
0	1	1	0	0	0	4.05 V
0	1	1	0	0	1	4.10 V
0	1	1	0	1	0	4.15 V
0	1	1	0	1	1	4.20 V
0	1	1	1	0	0	4.25 V
0	1	1	1	0	1	4.30 V
0	1	1	1	1	0	4.35 V
0	1	1	1	1	1	4.40 V

VRH [5:0]						GVDD
1	0	0	0	0	0	4.45 V
1	0	0	0	0	1	4.50 V
1	0	0	0	1	0	4.55 V
1	0	0	0	1	1	4.60 V
1	0	0	1	0	0	4.65 V
1	0	0	1	0	1	4.70 V
1	0	0	1	1	0	4.75 V
1	0	0	1	1	1	4.80 V
1	0	1	0	0	0	4.85 V
1	0	1	0	0	1	4.90 V
1	0	1	0	1	0	4.95 V
1	0	1	0	1	1	5.00 V
1	0	1	1	0	0	5.05 V
1	0	1	1	0	1	5.10 V
1	0	1	1	1	0	5.15 V
1	0	1	1	1	1	5.20 V
1	1	0	0	0	0	5.25 V
1	1	0	0	0	1	5.30 V
1	1	0	0	1	0	5.35 V
1	1	0	0	1	1	5.40 V
1	1	0	1	0	0	5.45 V
1	1	0	1	0	1	5.50 V
1	1	0	1	1	0	5.55 V
1	1	0	1	1	1	5.60 V
1	1	1	0	0	0	5.65 V
1	1	1	0	0	1	5.70 V
1	1	1	0	1	0	5.75 V
1	1	1	0	1	1	5.80 V
1	1	1	1	0	0	5.85 V
1	1	1	1	0	1	5.90 V
1	1	1	1	1	0	5.95 V
1	1	1	1	1	1	6.00 V

Note1: Make sure that VC and VRH setting restriction: GVDD ≦ (AVDD - 0.5) V.

VC [3:0]: Sets VCI1 regulator voltage.

VC [3:0]				VCI1 Voltage
0	0	0	0	2.30V
0	0	0	1	2.35V
0	0	1	0	2.40V
0	0	1	1	2.45V
0	1	0	0	2.50V
0	1	0	1	2.55V
0	1	1	0	2.60V
0	1	1	1	2.65V
1	0	0	0	2.70V
1	0	0	1	2.75V
1	0	1	0	2.80V
1	0	1	1	2.85V
1	1	0	0	2.90V
1	1	0	1	2.95V
1	1	1	0	3.00V
1	1	1	1	External VCI

Note: Do not set any higher VCI1 level than VCI - 0.2V.

<table>
<tr><td>Restriction</td><td>EXTC should be high to enable this command</td></tr>
<tr><td>Register
Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Sleep IN</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr>
<tr><th>VC [3:0]</th><th>VRH [5:0]</th></tr>
<tr><td>Power ON Sequence</td><td>4’b0000</td><td>6’h26h</td></tr>
<tr><td>SW Reset</td><td>4’b0000</td><td>6’h26h</td></tr>
<tr><td>HW Reset</td><td>4’b0000</td><td>6’h26h</td></tr>
</table>
</td></tr>
</table>

8.3.17. Power Control 2 (C1h)

C1h	PWCTRL 2 (Power Control 2)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	0	0	0	1	C1h
Parameter	1	1	↑	XX	0	0	0	0	BT [3:0]				00

Description

BT [3:0]: Sets the factor used in the step-up circuits.

Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.

BT [3:0]				AVDD	VGH	VGL
0	0	0	0	VCI1 x 2	VCI1 x 6	-VCI1 x 5
0	0	0	1			-VCI1 x 4
0	0	1	0			-VCI1 x 3
0	0	1	1		VCI1 x 5	-VCI1 x 5
0	1	0	0			-VCI1 x 4
0	1	0	1			-VCI1 x 3
0	1	1	0		VCI1 x 4	-VCI1 x 4
0	1	1	1			-VCI1 x 3
others				Setting Prohibited		

Note1: Make sure that AVDD setting restriction: AVDD ≦ 6.0 V.

2: Make sure that VGH and VGL setting restriction: VGH -VGL≦ 32 V.

Restriction: EXTC should be high to enable this command

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value
	BT [3:0]
Power ON Sequence	4'b0000
SW Reset	4'b0000
HW Reset	4'b0000

8.3.18. Power Control 3 (For Normal Mode) (C2h)

C2h	PWCTRL 3 (Power Control 3)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	0	0	1	0	C2h
Parameter	1	1	↑	XX	sync_opt 1	DCA1 [2:0]			sync_opt 0	DCA0 [2:0]			B2

Description

DCA0 [2:0]: Selects the operating frequency of the step-up circuit 1 for Normal mode. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

sync_opt 0: DC0A sync with line or frame

DCA1 [2:0]: Selects the operating frequency of the step-up circuit 2/3/4 for Normal mode. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

sync_opt 1: DC1A sync with line or frame.

DCA0 [2:0]			Step-up cycle for step-up circuit 1
0	0	0	fosc / 1
0	0	1	fosc / 2
0	1	0	fosc / 4
0	1	1	fosc / 8
1	0	0	fosc / 16
1	0	1	fosc / 32
1	1	0	fosc / 64
1	1	1	Setting prohibited

DCA1 [2:0]			Step-up cycle for step-up circuit 2/3/4
0	0	0	fosc / 2
0	0	1	fosc / 4
0	1	0	fosc / 8
0	1	1	fosc / 16
1	0	0	fosc / 32
1	0	1	fosc / 64
1	1	0	fosc / 128
1	1	1	Setting prohibited

Sync mode	**0**	**1**
sync_opt 0	Line sync	Frame sync
sync_opt 1		

Restriction: EXTC should be high to enable this command

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	DCA0 [2:0]	DCA1 [2:0]
Power ON Sequence	3'b010	3'b011
SW Reset	3'b010	3'b011
HW Reset	3'b010	3'b011

8.3.19. Power Control 4 (For Idle Mode) (C3h)

C3h	PWCTRL 4 (Power Control 4)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	0	0	1	1	C3h
Parameter	1	1	↑	XX	1	DCB1 [2:0]			0	DCB0 [2:0]			B2

Description

DCB0 [2:0]: Selects the operating frequency of the step-up circuit 1 for Idle mode. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DCB1 [2:0]: Selects the operating frequency of the step-up circuit 2/3/4 for Idle mode. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DCB0 [2:0]			Step-up cycle for step-up circuit 1
0	0	0	fosc / 1
0	0	1	fosc / 2
0	1	0	fosc / 4
0	1	1	fosc / 8
1	0	0	fosc / 16
1	0	1	fosc / 32
1	1	0	fosc / 64
1	1	1	Setting prohibited

DCB1 [2:0]			Step-up cycle for step-up circuit 2/3/4
0	0	0	fosc / 2
0	0	1	fosc / 4
0	1	0	fosc / 8
0	1	1	fosc / 16
1	0	0	fosc / 32
1	0	1	fosc / 64
1	1	0	fosc / 128
1	1	1	Setting prohibited

Restriction: EXTC should be high to enable this command

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	DCB0 [2:0]	DCB1 [2:0]
Power ON Sequence	3'b010	3'b011
SW Reset	3'b010	3'b011
H/W Reset	3'b010	3'b011

8.3.20. Power Control 5 (For Partial Mode) (C4h)

C4h	PWCTRL 5 (Power Control 5)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	0	1	0	0	C4h
Parameter	1	1	↑	XX	1	DCC1 [2:0]			0	DCC0 [2:0]			B2

Description

DCC0 [2:0]: Selects the operating frequency of the step-up circuit 1 for Partial mode. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DCC1 [2:0]: Selects the operating frequency of the step-up circuit 2/3/4 for Partial mode. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DCC0 [2:0]			Step-up cycle for step-up circuit 1
0	0	0	fosc / 1
0	0	1	fosc / 2
0	1	0	fosc / 4
0	1	1	fosc / 8
1	0	0	fosc / 16
1	0	1	fosc / 32
1	1	0	fosc / 64
1	1	1	Setting prohibited

DCC1 [2:0]			Step-up cycle for step-up circuit 2/3/4
0	0	0	fosc / 2
0	0	1	fosc / 4
0	1	0	fosc / 8
0	1	1	fosc / 16
1	0	0	fosc / 32
1	0	1	fosc / 64
1	1	0	fosc / 128
1	1	1	Setting prohibited

Restriction: EXTC should be high to enable this command

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	DCC0 [2:0]	DCC1 [2:0]
Power ON Sequence	3'b010	3'b011
SW Reset	3'b010	3'b011
HW Reset	3'b010	3'b011

8.3.21. VCOM Control 1(C5h)

C5h	VMCTRL1 (VCOM Control 1)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	0	1	0	1	C5h
1st Parameter	1	1	↑	XX	0	VMH [6:0]							31
2ndParameter	1	1	↑	XX	0	VML [6:0]							3C

Description

VMH [6:0] : Set the VCOMH voltage.

VMH [6:0]	VCOMH(V)	VMH [6:0]	VCOMH(V)	VMH [6:0]	VCOMH(V)	VMH [6:0]	VCOMH(V)
0000000	2.700	0100000	3.500	1000000	4.300	1100000	5.100
0000001	2.725	0100001	3.525	1000001	4.325	1100001	5.125
0000010	2.750	0100010	3.550	1000010	4.350	1100010	5.150
0000011	2.775	0100011	3.575	1000011	4.375	1100011	5.175
0000100	2.800	0100100	3.600	1000100	4.400	1100100	5.200
0000101	2.825	0100101	3.625	1000101	4.425	1100101	5.225
0000110	2.850	0100110	3.650	1000110	4.450	1100110	5.250
0000111	2.875	0100111	3.675	1000111	4.475	1100111	5.275
0001000	2.900	0101000	3.700	1001000	4.500	1101000	5.300
0001001	2.925	0101001	3.725	1001001	4.525	1101001	5.325
0001010	2.950	0101010	3.750	1001010	4.550	1101010	5.350
0001011	2.975	0101011	3.775	1001011	4.575	1101011	5.375
0001100	3.000	0101100	3.800	1001100	4.600	1101100	5.400
0001101	3.025	0101101	3.825	1001101	4.625	1101101	5.425
0001110	3.050	0101110	3.850	1001110	4.650	1101110	5.450
0001111	3.075	0101111	3.875	1001111	4.675	1101111	5.475
0010000	3.100	0110000	3.900	1010000	4.700	1110000	5.500
0010001	3.125	0110001	3.925	1010001	4.725	1110001	5.525
0010010	3.150	0110010	3.950	1010010	4.750	1110010	5.550
0010011	3.175	0110011	3.975	1010011	4.775	1110011	5.575
0010100	3.200	0110100	4.000	1010100	4.800	1110100	5.600
0010101	3.225	0110101	4.025	1010101	4.825	1110101	5.625
0010110	3.250	0110110	4.050	1010110	4.850	1110110	5.650
0010111	3.275	0110111	4.075	1010111	4.875	1110111	5.675
0011000	3.300	0111000	4.100	1011000	4.900	1111000	5.700
0011001	3.325	0111001	4.125	1011001	4.925	1111001	5.725
0011010	3.350	0111010	4.150	1011010	4.950	1111010	5.750
0011011	3.375	0111011	4.175	1011011	4.975	1111011	5.775
0011100	3.400	0111100	4.200	1011100	5.000	1111100	5.800
0011101	3.425	0111101	4.225	1011101	5.025	1111101	5.825
0011110	3.450	0111110	4.250	1011110	5.050	1111110	5.850
0011111	3.475	0111111	4.275	1011111	5.075	1111111	5.875

VML [6:0] : Set the VCOML voltage

VML [6:0]	VCOML(V)	VML [6:0]	VCOML(V)	VML [6:0]	VCOML(V)	VML [6:0]	VCOML(V)
0000000	-2.500	0100000	-1.700	1000000	-0.900	1100000	-0.100
0000001	-2.475	0100001	-1.675	1000001	-0.875	1100001	-0.075
0000010	-2.450	0100010	-1.650	1000010	-0.850	1100010	-0.050
0000011	-2.425	0100011	-1.625	1000011	-0.825	1100011	-0.025
0000100	-2.400	0100100	-1.600	1000100	-0.800	1100100	0
0000101	-2.375	0100101	-1.575	1000101	-0.775	1100101	Reserved
0000110	-2.350	0100110	-1.550	1000110	-0.750	1100110	Reserved
0000111	-2.325	0100111	-1.525	1000111	-0.725	1100111	Reserved
0001000	-2.300	0101000	-1.500	1001000	-0.700	1101000	Reserved
0001001	-2.275	0101001	-1.475	1001001	-0.675	1101001	Reserved
0001010	-2.250	0101010	-1.450	1001010	-0.650	1101010	Reserved
0001011	-2.225	0101011	-1.425	1001011	-0.625	1101011	Reserved
0001100	-2.200	0101100	-1.400	1001100	-0.600	1101100	Reserved
0001101	-2.175	0101101	-1.375	1001101	-0.575	1101101	Reserved
0001110	-2.150	0101110	-1.350	1001110	-0.550	1101110	Reserved
0001111	-2.125	0101111	-1.325	1001111	-0.525	1101111	Reserved
0010000	-2.100	0110000	-1.300	1010000	-0.500	1110000	Reserved
0010001	-2.075	0110001	-1.275	1010001	-0.475	1110001	Reserved
0010010	-2.050	0110010	-1.250	1010010	-0.450	1110010	Reserved
0010011	-2.025	0110011	-1.225	1010011	-0.425	1110011	Reserved

0010100	-2.000	0110100	-1.200	1010100	-0.400	1110100	Reserved
0010101	-1.975	0110101	-1.175	1010101	-0.375	1110101	Reserved
0010110	-1.950	0110110	-1.150	1010110	-0.350	1110110	Reserved
0010111	-1.925	0110111	-1.125	1010111	-0.325	1110111	Reserved
0011000	-1.900	0111000	-1.100	1011000	-0.300	1111000	Reserved
0011001	-1.875	0111001	-1.075	1011001	-0.275	1111001	Reserved
0011010	-1.850	0111010	-1.050	1011010	-0.250	1111010	Reserved
0011011	-1.825	0111011	-1.025	1011011	-0.225	1111011	Reserved
0011100	-1.800	0111100	-1.000	1011100	-0.200	1111100	Reserved
0011101	-1.775	0111101	-0.975	1011101	-0.175	1111101	Reserved
0011110	-1.750	0111110	-0.950	1011110	-0.150	1111110	Reserved
0011111	-1.725	0111111	-0.925	1011111	-0.125	1111111	Reserved

Restriction: EXTC should be high to enable this command

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	VMH [6:0]	VML [6:0]
Power ON Sequence	7'h31	7'h3C
SW Reset	7'h31	7'h3C
HW Rest	7'h31	7'h3C

8.3.22. VCOM Control 2(C7h)

C7h	VMCTRL1 (VCOM Control 1)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	0	1	1	1	C7h
Parameter	1	1	↑	XX	nVM	VMF [6:0]							C0

Description

nVM: nVM equals to "0" after power on reset and VCOM offset equals to program MTP value. When nVM set to "1", setting of VMF [6:0] becomes valid and VCOMH/VCOML can be adjusted.

VMF [6:0]: Set the VCOM offset voltage.

VMF[6:0]	VCOMH	VCOML
0000000	VMH	VML
0000001	VMH – 63	VML – 63
0000010	VMH – 62	VML – 62
0000011	VMH – 61	VML – 61
0000100	VMH – 60	VML – 60
0000101	VMH – 58	VML – 58
0000110	VMH – 58	VML – 58
0000111	VMH – 57	VML – 57
0001000	VMH – 56	VML – 56
0001001	VMH – 55	VML – 55
0001010	VMH – 54	VML – 54
0001011	VMH – 53	VML – 53
0001100	VMH – 52	VML – 52
0001101	VMH – 51	VML -51
0001110	VMH – 50	VML – 50
0001111	VMH – 49	VML – 49
0010000	VMH – 48	VML – 48
0010001	VMH – 47	VML – 47
0010010	VMH – 46	VML – 46
0010011	VMH – 45	VML – 45
0010100	VMH – 44	VML – 44
0010101	VMH – 43	VML – 43
0010110	VMH – 42	VML – 42
0010111	VMH – 41	VML – 41
0011000	VMH – 40	VML – 40
0011001	VMH – 39	VML – 39
0011010	VMH – 38	VML – 38
0011011	VMH – 37	VML – 37
0011100	VMH – 36	VML – 36
0011101	VMH – 35	VML – 35
0011110	VMH – 34	VML – 34
0011111	VMH – 33	VML – 33
0100000	VMH – 32	VML – 32
0100001	VMH – 31	VML – 31
0100010	VMH – 30	VML – 30
0100011	VMH – 29	VML – 29
0100100	VMH – 28	VML – 28
0100101	VMH – 27	VML – 27
0100110	VMH – 26	VML – 26
0100111	VMH – 25	VML – 25
0101000	VMH – 24	VML – 24
0101001	VMH – 23	VML – 23
0101010	VMH – 22	VML – 22
0101011	VMH – 21	VML – 21
0101100	VMH – 20	VML – 20
0101101	VMH – 19	VML – 19
0101110	VMH – 18	VML – 18
0101111	VMH – 17	VML – 17
0110000	VMH – 16	VML – 16
0110001	VMH – 15	VML – 15
0110010	VMH – 14	VML – 14
0110011	VMH – 13	VML – 13

VMF[6:0]	VCOMH	VCOML
1000000	VMH	VML
1000001	VMH + 1	VML + 1
1000010	VMH + 2	VML + 2
1000011	VMH + 3	VML + 3
1000100	VMH + 4	VML + 4
1000101	VMH + 5	VML + 5
1000110	VMH + 6	VML + 6
1000111	VMH + 7	VML + 7
1001000	VMH + 8	VML + 8
1001001	VMH + 9	VML + 9
1001010	VMH + 10	VML + 10
1001011	VMH + 11	VML + 11
1001100	VMH + 12	VML + 12
1001101	VMH + 13	VML + 13
1001110	VMH + 14	VML + 14
1001111	VMH + 15	VML + 15
1010000	VMH + 16	VML + 16
1010001	VMH + 17	VML + 17
1010010	VMH + 18	VML + 18
1010011	VMH + 19	VML + 19
1010100	VMH + 20	VML + 20
1010101	VMH + 21	VML + 21
1010110	VMH + 22	VML + 22
1010111	VMH + 23	VML + 23
1011000	VMH + 24	VML + 24
1011001	VMH + 25	VML + 25
1011010	VMH + 26	VML + 26
1011011	VMH + 27	VML + 27
1011100	VMH + 28	VML + 28
1011101	VMH + 29	VML + 29
1011110	VMH + 30	VML + 30
1011111	VMH + 31	VML + 31
1100000	VMH + 32	VML + 32
1100001	VMH + 33	VML + 33
1100010	VMH + 34	VML + 34
1100011	VMH + 35	VML + 35
1100100	VMH + 36	VML + 36
1100101	VMH + 37	VML + 37
1100110	VMH + 38	VML + 38
1100111	VMH + 39	VML + 39
1101000	VMH + 40	VML + 40
1101001	VMH + 41	VML + 41
1101010	VMH + 42	VML + 42
1101011	VMH + 43	VML + 43
1101100	VMH + 44	VML + 44
1101101	VMH + 45	VML + 45
1101110	VMH + 46	VML + 46
1101111	VMH + 47	VML + 47
1110000	VMH + 48	VML + 48
1110001	VMH + 49	VML + 49
1110010	VMH + 50	VML + 50
1110011	VMH + 51	VML + 51

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<tr><td></td><td>
<table>
<tr><td>0110100</td><td>VMH – 12</td><td>VML – 12</td><td></td><td>1110100</td><td>VMH + 52</td><td>VML + 52</td></tr>
<tr><td>0110101</td><td>VMH – 11</td><td>VML – 11</td><td></td><td>1110101</td><td>VMH + 53</td><td>VML + 53</td></tr>
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<tr><td>0110111</td><td>VMH – 9</td><td>VML – 9</td><td></td><td>1110111</td><td>VMH + 55</td><td>VML + 55</td></tr>
<tr><td>0111000</td><td>VMH – 8</td><td>VML – 8</td><td></td><td>1111000</td><td>VMH + 56</td><td>VML + 56</td></tr>
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<tr><td>0111010</td><td>VMH – 6</td><td>VML – 6</td><td></td><td>1111010</td><td>VMH + 58</td><td>VML + 58</td></tr>
<tr><td>0111011</td><td>VMH – 5</td><td>VML – 5</td><td></td><td>1111011</td><td>VMH + 59</td><td>VML + 59</td></tr>
<tr><td>0111100</td><td>VMH – 4</td><td>VML – 4</td><td></td><td>1111100</td><td>VMH + 60</td><td>VML + 60</td></tr>
<tr><td>0111101</td><td>VMH – 3</td><td>VML – 3</td><td></td><td>1111101</td><td>VMH + 61</td><td>VML + 61</td></tr>
<tr><td>0111110</td><td>VMH – 2</td><td>VML – 2</td><td></td><td>1111110</td><td>VMH + 62</td><td>VML + 62</td></tr>
<tr><td>0111111</td><td>VMH – 1</td><td>VML – 1</td><td></td><td>1111111</td><td>VMH + 63</td><td>VML + 63</td></tr>
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<tr><td>Restriction</td><td>EXTC should be high to enable this command</td></tr>
<tr><td>Register Availability</td><td>
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<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Sleep IN</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr>
<tr><th>nVM</th><th>VMF [6:0]</th></tr>
<tr><td>Power ON Sequence</td><td>1’b1</td><td>7’h40h</td></tr>
<tr><td>SW Reset</td><td>1’b1</td><td>7’h40h</td></tr>
<tr><td>HW Reset</td><td>1’b1</td><td>7’h40h</td></tr>
</table>
</td></tr>
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8.3.23. NV Memory Write (D0h)

D0h	NVMWR (NV Memory Write)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	0	0	0	0	D0h
1st Parameter	1	1	↑	XX	0	0	0	0	0	PGM_ADR [2:0]			00
2ndParameter	1	1	↑	XX	PGM_DATA [7:0]								XX

Description

This command is used to program the NV memory data. After a successful MTP operation, the information of PGM_DATA [7:0] will programmed to NV memory.

PGM_ADR [2:0]: The select bits of ID1, ID2, ID3 and VMF [6:0] programming.

PGM_ADR [2:0]			Programmed NV Memory Selection
0	0	0	ID1 programming
0	0	1	ID2 programming
0	1	0	ID3 programming
1	0	0	VMF [6:0] programming
Others			Reserved

PGM_DATA [7:0]: The programmed data.

Restriction

EXTC should be high to enable this command

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	PGM_ADR [2:0]	PGM_DATA [7:0]
Power ON Sequence	3'b000	MTP value
SW Reset	3'b000	MTP value
HW Reset	3'b000	MTP value

8.3.24. NV Memory Protection Key (D1h)

D1h	NVMPKEY (NV Memory Protection Key)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	0	0	0	1	D1h
1st Parameter	1	1	↑	XX	KEY [23:16]								55h
2nd Parameter	1	1	↑	XX	KEY [15:8]								AAh
3rd Parameter	1	1	↑	XX	KEY [7:0]								66h
Description	**KEY [23:0]:** NV memory programming protection key. When writing MTP data to D1h, this register must be set to 0x55AA66h to enable MTP programming. If D1h register is not written with 0x55AA66h, then NV memory programming will be aborted.												
Restriction	EXTC should be high to enable this command												

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value
Power ON Sequence	KEY [23:0]=55AA66h
SW Reset	KEY [23:0]=55AA66h
HW Reset	KEY [23:0]=55AA66h

8.3.25. NV Memory Status Read (D2h)

D2h	RDNVM (NV Memory Status Read)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	0	0	1	0	D2h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2ndParameter	1	↑	1	XX	0	ID2_CNT [2:0]			0	ID1_CNT [2:0]			XX
3rdParameter	1	↑	1	XX	BUSY	VMF_CNT [2:0]			0	ID3_CNT [2:0]			XX

Description

ID1_CNT [2:0] / **ID2_CNT [2:0]** / **ID3_CNT [2:0]** / **VMF_CNT [2:0]:** NV memory program record. The bits will increase "+1" automatically after writing the PGM_DATA [7:0] to NV memory.

ID1_CNT [2:0] / ID2_CNT [2:0] ID3_CNT [2:0] / VMF_CNT [2:0]			Description
Status			Availability
0	0	0	No Programmed
0	0	1	Programmed 1 time
0	1	1	Programmed 2 times
1	1	1	Programmed 3 times

BUSY: The status bit of NV memory programming.

BUSY	The Status of NV Memory
0	Idle
1	Busy

Restriction

EXTC should be high to enable this command

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value				
	ID3_CNT	ID2_CNT	ID1_CNT	VMF_CNT	BUSY
Power ON Sequence	X	X	X	X	X
SW Reset	X	X	X	X	X
HW Reset	X	X	X	X	X

8.3.26. Read ID4 (D3h)

D3h	RDID4 (Read ID4)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	0	0	1	1	D3h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
2ndParameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
3rdParameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
4th Parameter	1	↑	1	XX	0	1	0	0	0	0	0	0	40h
Description	Read IC device code. The 1st parameter is dummy read period. The 4th parameter mean the IC model name.												
Restriction	EXTC should be high to enable this command												

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value
Power ON Sequence	24'hXXXX40h
SW Reset	24'hXXXX40h
HW Reset	24'hXXXX40h

8.3.27. Positive Gamma Correction (E0h)

E0h	PGAMCTRL (Positive Gamma Control)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	0	0	0	0	0	E0h
1st Parameter	1	1	↑	XX	X	X	X	X	VP63 [3:0]				0F
2ndParameter	1	1	↑	XX	X	X	VP62 [5:0]						22
3rdParameter	1	1	↑	XX	X	X	VP61 [5:0]						1F
4th Parameter	1	1	↑	X	X	X	X	X	VP59 [3:0]				0A
5th Parameter	1	1	↑	XX	X	X	X	VP57 [4:0]					0E
6th Parameter	1	1	↑	XX	X	X	X	X	VP50 [3:0]				06
7th Parameter	1	1	↑	XX	X	VP43 [6:0]							4D
8th Parameter	1	1	↑	XX	VP27 [3:0]				VP36 [3:0]				76
9th Parameter	1	1	↑	XX	X	VP20 [6:0]							3B
10thParameter	1	1	↑	XX	X	X	X	X	VP13 [3:0]				03
11thParameter	1	1	↑	XX	X	X	X	VP6 [4:0]					0E
12thParameter	1	1	↑	XX	X	X	X	X	VP4 [3:0]				04
13thParameter	1	1	↑	XX	X	X	VP2 [5:0]						13
14thParameter	1	1	↑	XX	X	XX	VP1 [5:0]						0E
15thParameter	1	1	↑	XX	X	X	X	X	VP0 [3:0]				0C
Description	Set the gray scale voltage to adjust the gamma characteristics of the TFT panel. VP0 is the maximum Gamma output voltage in positive polarity. VP63 is the minimum Gamma output voltage in positive polarity.												
Restriction	EXTC should be high to enable this command												
Register Availability													
Default													

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

8.3.28. Negative Gamma Correction (E1h)

E1h	NGAMCTRL (Negative Gamma Correction)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	0	0	0	0	1	E1h
1st Parameter	1	1	↑	XX	X	X	X	X	VN0 [3:0]				0C
2ndParameter	1	1	↑	XX	X	X	VN1 [5:0]						23
3rdParameter	1	1	↑	XX	X	X	VN2 [5:0]						26
4th Parameter	1	1	↑	XX	X	X	X	X	VN4 [3:0]				04
5th Parameter	1	1	↑	XX	X	X	X	VN6 [4:0]					10
6th Parameter	1	1	↑	XX	X	X	X	X	VN13 [3:0]				04
7th Parameter	1	1	↑	XX	X	VN20 [6:0]							39
8th Parameter	1	1	↑	XX	VN36 [3:0]				VN27 [3:0]				24
9th Parameter	1	1	↑	XX	X	VN43 [6:0]							4B
10thParameter	1	1	↑	XX	X	X	X	X	VN50 [3:0]				03
11thParameter	1	1	↑	XX	X	X	X	VN57 [4:0]					0B
12thParameter	1	1	↑	XX	X	X	X	X	VN59 [3:0]				0B
13thParameter	1	1	↑	XX	X	X	VN61 [5:0]						33
14thParameter	1	1	↑	XX	X	X	VN62 [5:0]						37
15thParameter	1	1	↑	XX	X	X	X	X	VN63 [3:0]				0F
Description	Set the gray scale voltage to adjust the gamma characteristics of the TFT panel. VN63is the maximum Gamma output voltage in negative polarity. VN0 is the minimum Gamma output voltage in negative polarity.												
Restriction	EXTC should be high to enable this command												
Register Availability													
Default													

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

8.3.29. Digital Gamma Control 1 (E2h)

E2h	DGAMCTRL (Digital Gamma Control 1)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	0	0	0	1	0	E2h
1st Parameter	1	1	↑	XX	RCA0 [3:0]				BCA0 [3:0]				XX
:	1	1	↑	XX	RCAx [3:0]				BCAx [3:0]				XX
16th Parameter	1	1	↑	XX	RCA15 [3:0]				BCA15 [3:0]				XX
Description	**RCAx [3:0]:** Gamma Macro-adjustment registers for red gamma curve. **BCAx [3:0]:** Gamma Macro-adjustment registers for blue gamma curve.												
Restriction	EXTC should be high to enable this command												

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	RCAx [3:0]	BCAx [3:0]
Power ON Sequence	TBD	TBD
SW Reset	TBD	TBD
HW Reset	TBD	TBD

8.3.30. Digital Gamma Control 2(E3h)

E3h	DGAMCTRL (Digital Gamma Control 2)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	0	0	0	1	1	E3h
1st Parameter	1	1	↑	XX	RFA0 [3:0]				BFA0 [3:0]				XX
:	1	1	↑	XX	RFAx [3:0]				BFAx [3:0]				XX
64rdParameter	1	1	↑	XX	RFA63 [3:0]				BFA63 [3:0]				XX
Description	**RFAx [3:0]:** Gamma Micro-adjustment register for red gamma curve. **BFAx [3:0]:** Gamma Micro-adjustment register for blue gamma curve.												
Restriction	EXTC should be high to enable this command												
Register Availability													

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	RFAx [3:0]	BFAx [3:0]
Power ON Sequence	TBD	TBD
SW Reset	TBD	TBD
HW Reset	TBD	TBD

8.3.31. 3-Gamma Control (F2h)

E3h	3GAMCTRL (3 Gamma Control)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	1	0	0	1	0	F2h
1st Parameter	1	1	↑	XX	X	X	X	X	X	X	En_dith	En_3g	10
Description	En_3g: Enable bit for 3-Gamma function.. En_dith: Enable bit for dithering function..												
Restriction	EXTC should be high to enable this command												
Register Availability													

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	En_dith	En_3g
Power ON Sequence	1'b1	1'b0
SW Reset	1'b1	1'b0
HW Reset	1'b1	1'b0

8.3.32. Interface Control (F6h)

F6h	IFCTL (16bits Data Format Selection)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	1	0	1	1	0	F6h
1st Parameter	1	1	↑	XX	MY_ EOR	MX_ EOR	MV_ EOR	0	BGR_ EOR	0	0	WE MODE	01
2nd Parameter	1	1	↑	XX	0	0	EPF [1]	EPF [0]	0	0	MDT [1]	MDT [0]	00
3rd Parameter	1	1	↑	XX	0	0	ENDIAN	0	DM [1]	DM [0]	RM	RIM	00

Description

MY_EOR / MX_EOR / MV_EOR / BGR_EOR:

The set value of MADCTL is used in the IC is derived as exclusive OR between 1st Parameter of IFCTL and MADCTL Parameter.

MDT [1:0]: Select the method of display data transferring.

WEMODE: Memory write control

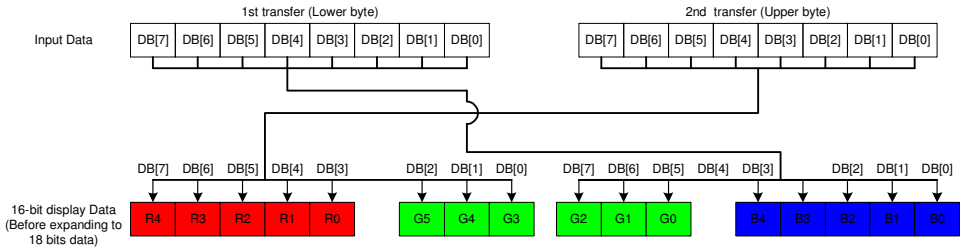
WEMODE=0: When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the exceeding data will be ignored.

WEMODE=1: When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the column and page number will be reset, and the exceeding data will be written into the following column and page.

ENDIAN: Select Little Endian Interface bit. At Little Endian mode, the host sends LSB data first.

ENDIAN	Data transfer Mode
0	Normal (MSB first, default)
1	Little Endian (LSB first)

Note: Little Endian is valid on only 65K 8-bit and 9-bit MCU interface mode.



DM [1:0]: Select the display operation mode.

DM [1]	DM [0]	Display Operation Mode
0	0	Internal clock operation
0	1	RGB Interface Mode
1	0	VSYNC interface mode
1	1	Setting disabled

The DM [1:0] setting allows switching between internal clock operation mode and external display interface operation mode.

However, switching between the RGB interface operation mode and the VSYNC interface operation mode is prohibited.

RM: Select the interface to access the GRAM.

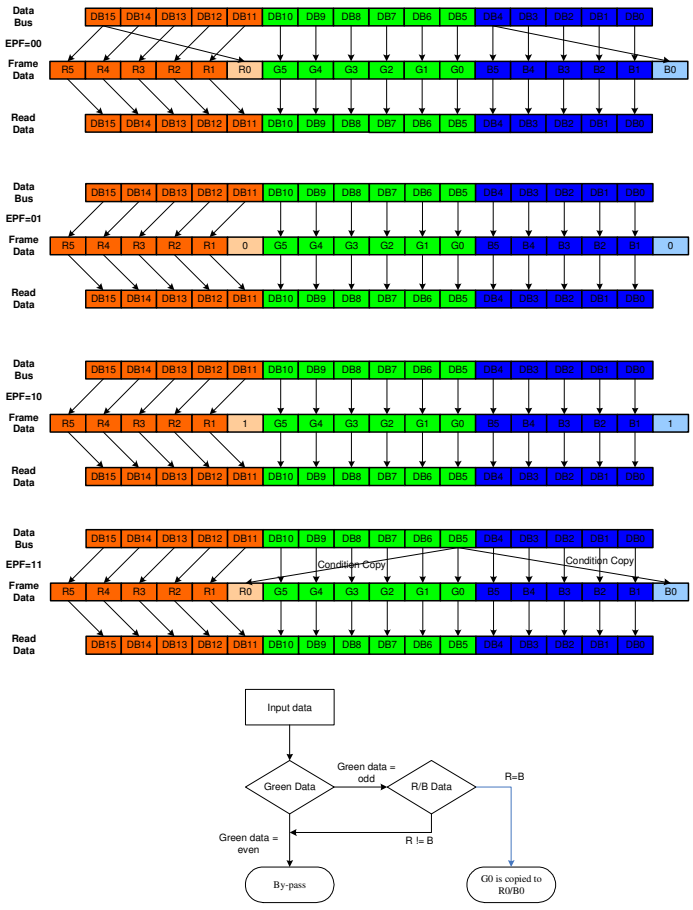
Set RM to "1" when writing display data by the RGB interface.

RM	Interface for RAM Access
0	System interface/VSYNC interface
1	RGB interface

RIM: Specify the RGB interface mode when the RGB interface is used. These bits should be set before display operation through the RGB interface and should not be set during operation.

RIM	COLMOD [6:4]	RGB Interface Mode
0	110 (262K color)	18- bit RGB interface (1 transfer/pixel)
	101 (65K color)	16- bit RGB interface (1 transfer/pixel)
1	110 (262K color)	6- bit RGB interface (3 transfer/pixel)
	101 (65K color)	6- bit RGB interface (3 transfer/pixel)

EPF [1:0]: 65K color mode data format.



EPF [1:0]	Expand 16 bbp (R,G,B) to 18bbp (R,G,B)
00	MSB is inputted to LSB r [5:0] = {R [4:0], R [4]} g [5:0] = {G [5:0]} b [5:0] = {B [4:0], B [4]}

	01	"0" is inputted to LSB r [5:0] = {R [4:0], 0} g [5:0] = {G [5:0]} b [5:0] = {B [4:0], 0} Exception: R [4:0], B[4:0] = 5'h1F → r [5:0], b[5:0] = 6'h3F
	10	"1" is inputted to LSB r [5:0] = {R [4:0], 1} g [5:0] = {G [5:0]} b [5:0] = {B [4:0], 1} Exception: R [4:0], B[4:0] = 5'h00 → r [5:0], b[5:0] = 6'h00
	11	Compare R [4:0], G [5:1], B [4:0] case: Case 1: R=G=B → r [5:0] = {R [4:0], G [0]}, g [5:0] = {G [5:0]}, b [5:0] = {B [4:0], G [0]} Case 2: R=B≠G → r [5:0] = {R [4:0], R [4]}, g [5:0] = {G [5:0]}, b [5:0] = {B [4:0], B [0]} Case 3: R=G≠B → r [5:0] = {R [4:0], G [0]}, g [5:0] = {G [5:0]}, b [5:0] = {B [4:0], B [0]} Case 4: B=G≠R → r [5:0] = {R [4:0], R [4]}, g [5:0] = {G [5:0]}, b [5:0] = {B [4:0], G [0]}

Restriction: EXTC should be high to enable this command

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

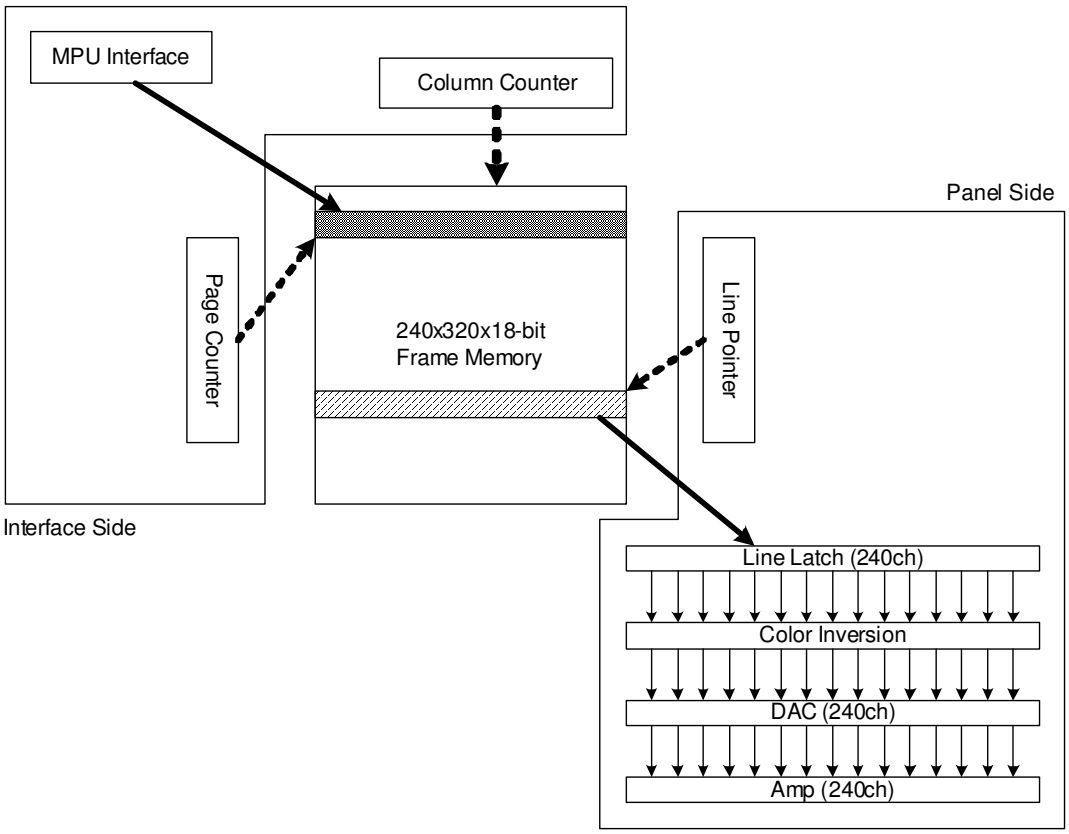
Default

Status	Default Value						
	EPF [1:0]	MDT [1:0]	ENDIAN	WEMODE	DM [1:0]	RM	RIM
Power ON Sequence	2'b00	2'b00	1'b0	1'b1	2'b00	1'b0	1'b0
SW Reset	2'b00	2'b00	1'b0	1'b1	2'b00	1'b0	1'b0
HW Reset	2'b00	2'b00	1'b0	1'b1	2'b00	1'b0	1'b0

9. Display Data RAM

9.1. Configuration

The display data RAM stores display dots and consists of 1,382,400 bits (240x18x320 bits). There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC. There will be no abnormal visible effect on the display when there is a simultaneous panel read and interface read or write display data to the same location of the frame memory.

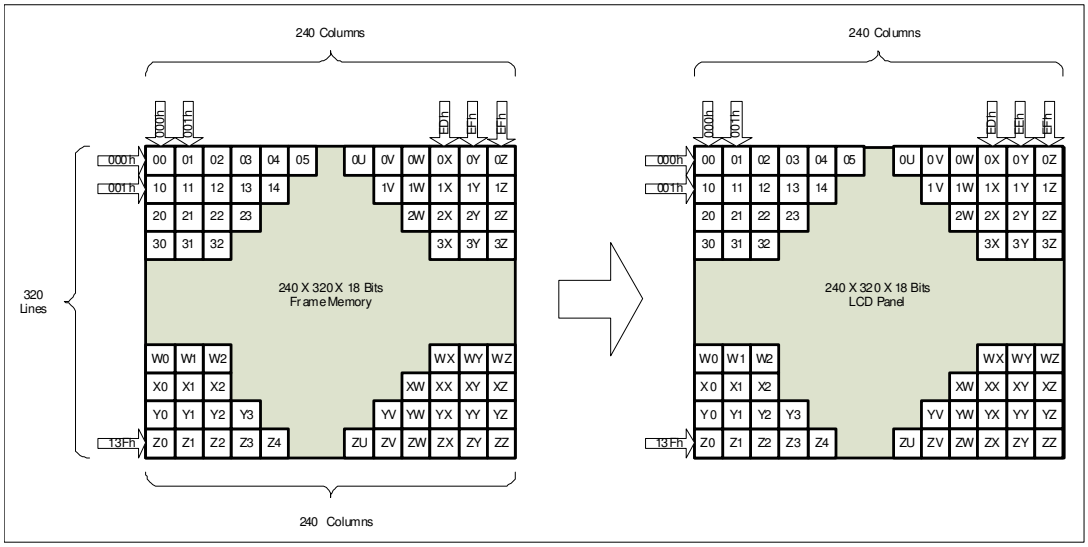


9.2. Memory to Display Address Mapping

9.2.1. Normal Display ON or Partial Mode ON, Vertical Scroll Mode OFF

In this mode, the content of frame memory within an area where column pointer is 0000h to 00EFh and page pointer is 0000h to 013Fh is displayed.

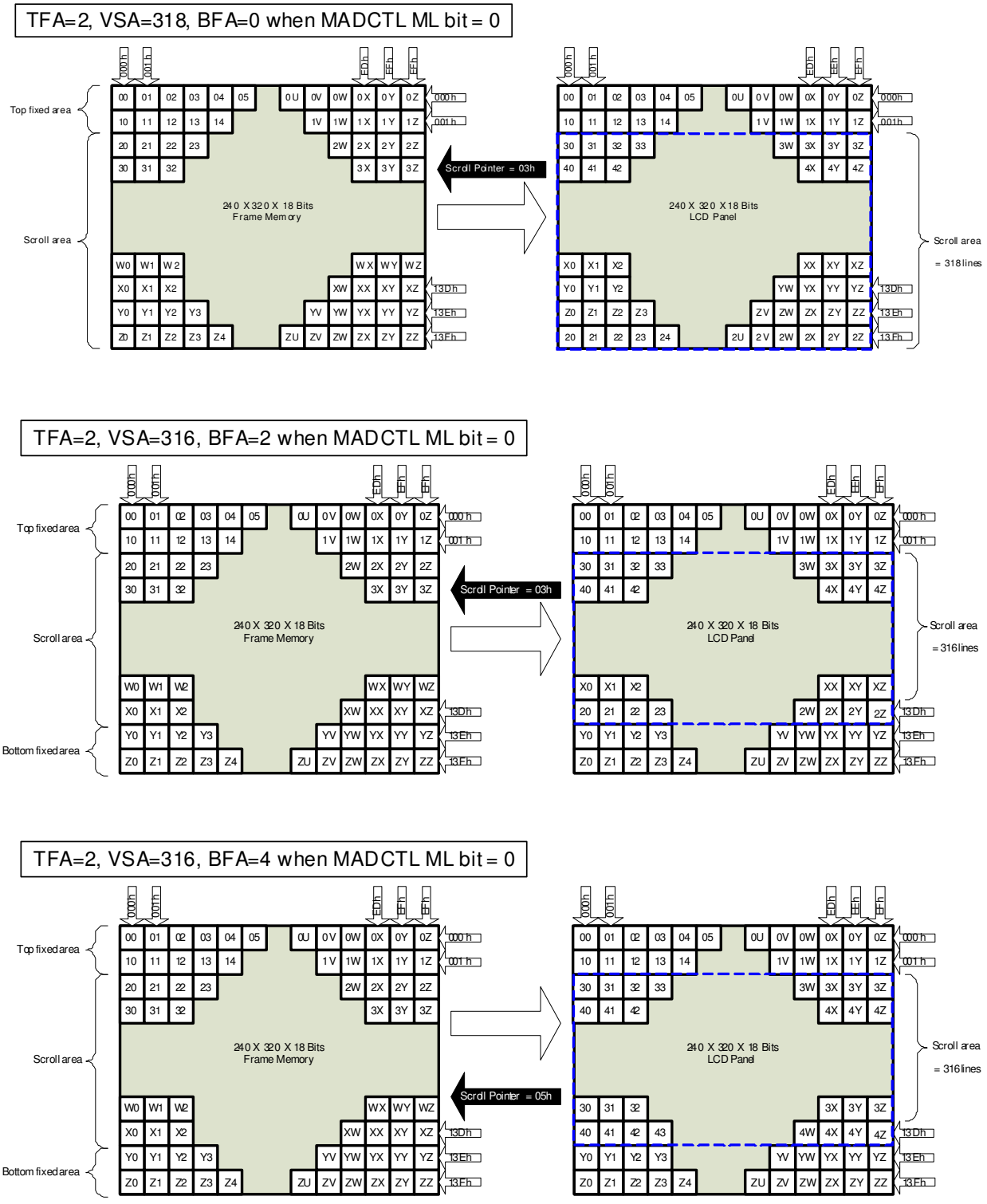
To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0, 0)



9.2.2. Vertical Scroll Mode

There is a vertical scrolling mode, which is determined by the commands “Vertical Scrolling Definition” (33h) and “Vertical Scrolling Start Address” (37h).

The Vertical Scroll Mode function is explained by these examples in the following.



Note: When Vertical Scrolling Definition Parameters (TFA+VSA+BFA) ≠ 320, Scrolling Mode is undefined.

9.2.3. Vertical Scroll Example

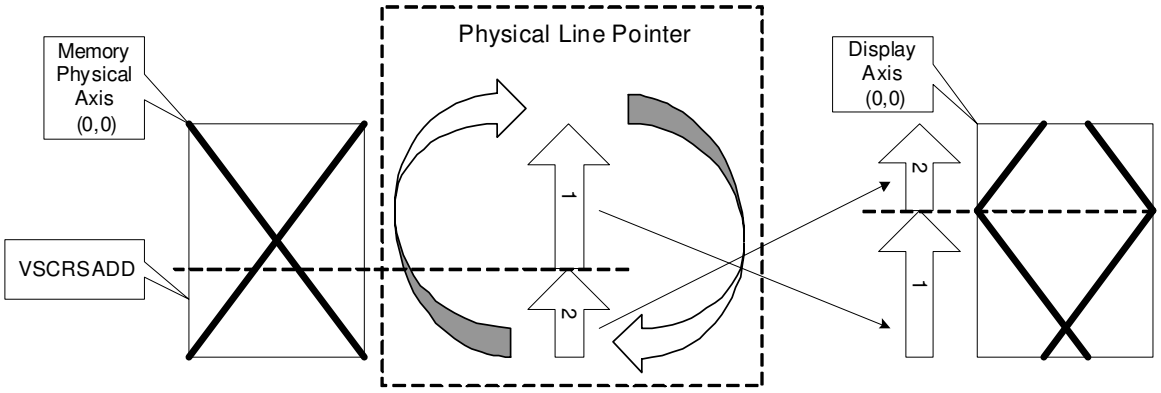
9.2.4. Case1: TFA+VSA+BFA < 320

This setting is prohibited, unless unexpected picture will be shown.

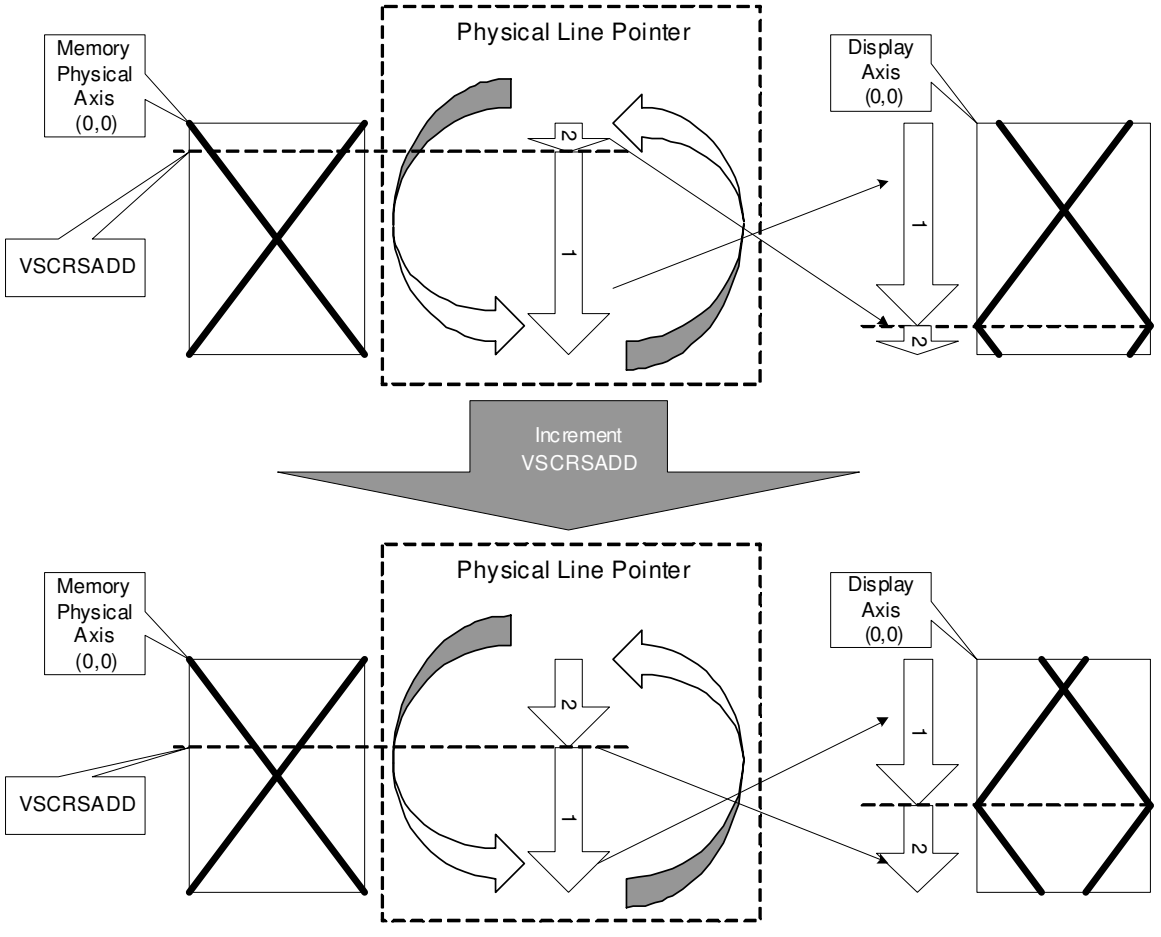
9.2.5. Case2: TFA+VSA+BFA = 320 (Rolling Scrolling)

The operation of Rolling Scrolling is explained by these examples in the following.

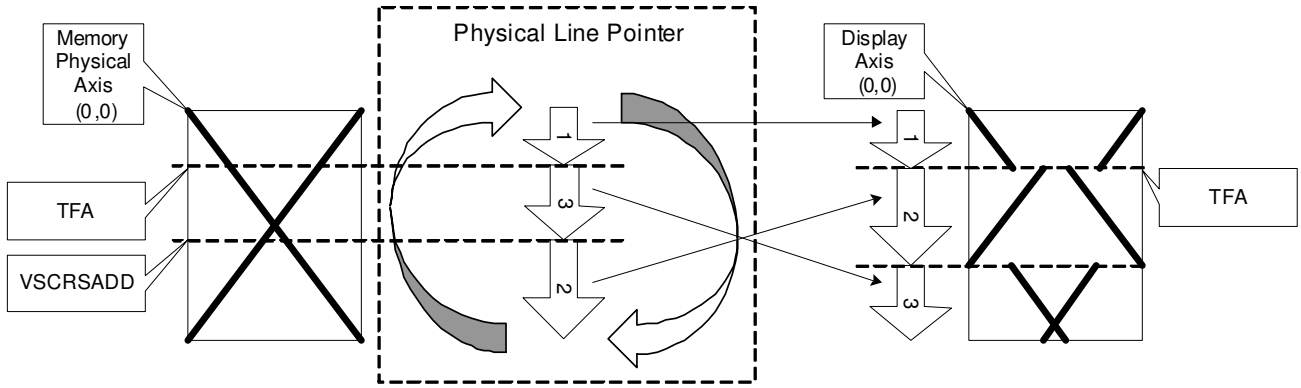
When TFA=0, VSA=320, BFA=0, VSCRSADD=40 and MADCTL ML bit = 1



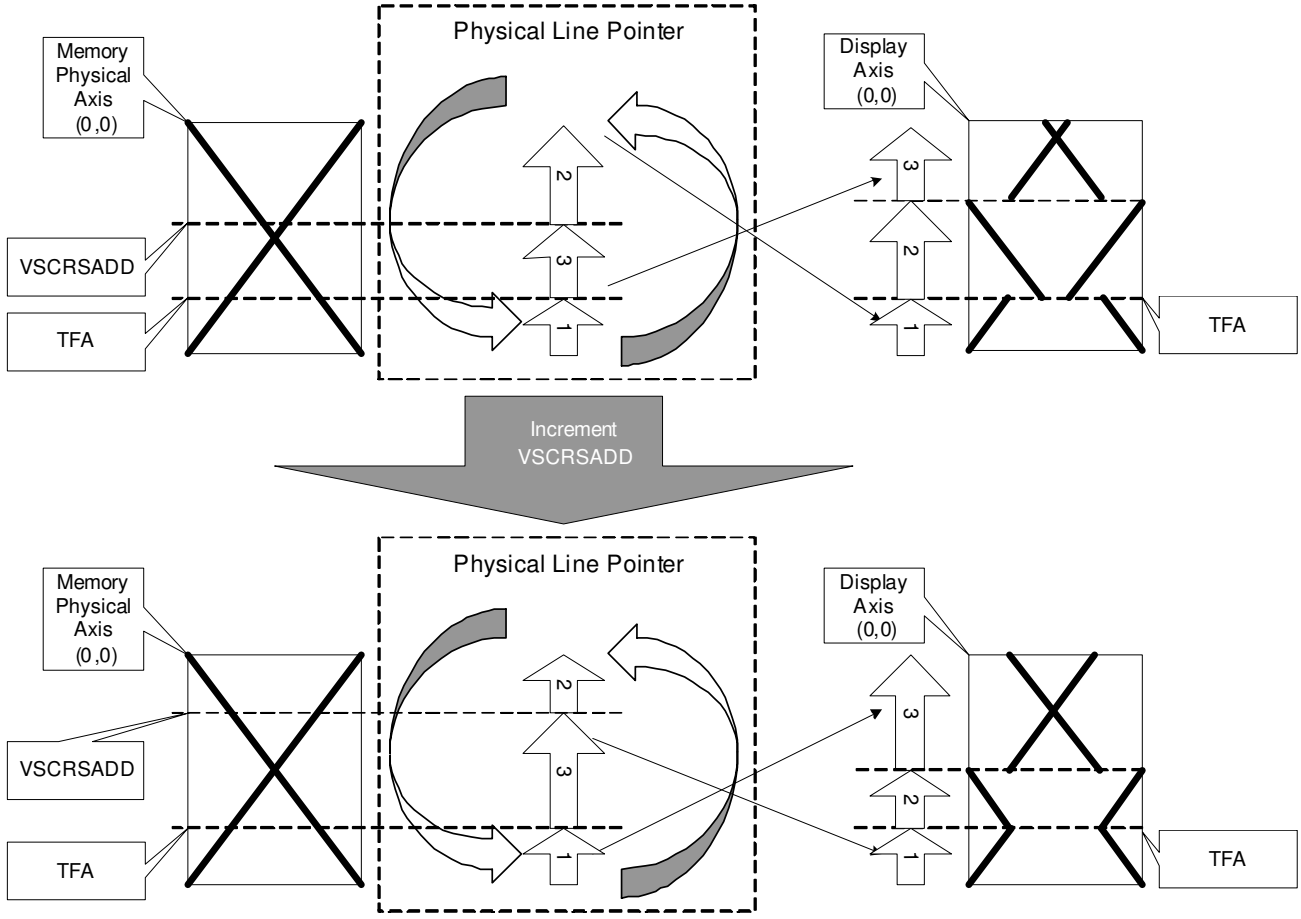
When TFA=0, VSA=320, BFA=0, VSCRSADD=40 and MADCTL ML bit = 0



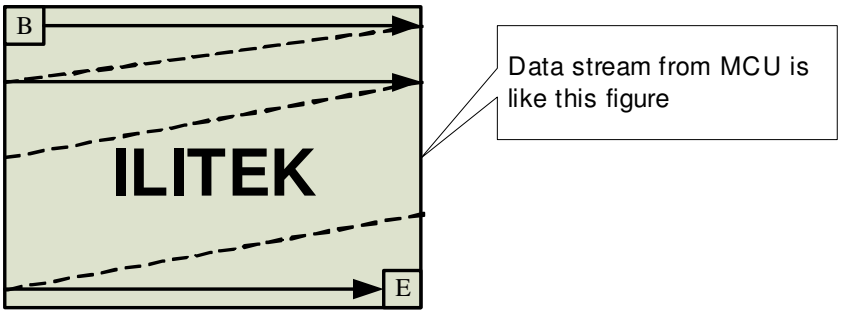
When TFA=30, VSA=290, BFA=0, VSCRSADD=80 and MADCTL ML bit = 0



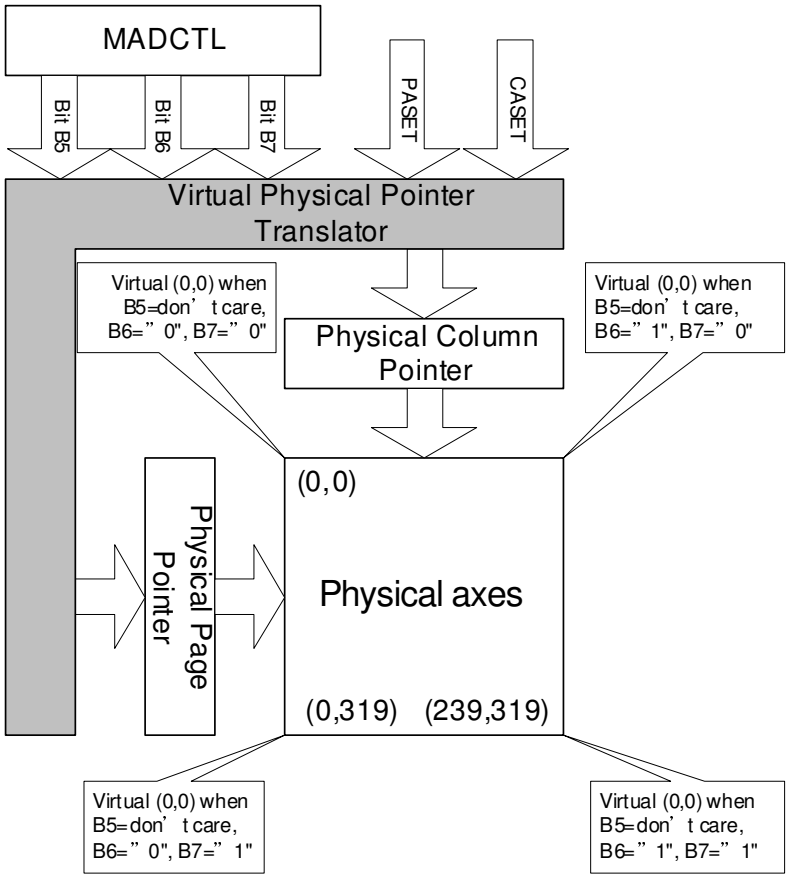
When TFA=30, VSA=290, BFA=0, VSCRSADD=80 and MADCTL ML bit = 1



9.3. MCU to memory write/read direction



The data is written in the order illustrated above. The Counter which dictates where in the physical memory the data is to be written is controlled by “Memory Data Access Control” Command, Bits B5, B6, and B7 as described below.



B5	B6	B7	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (319-Physical Page Pointer)
0	1	0	Direct to (239-Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (239-Physical Column Pointer)	Direct to (319-Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (319-Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (239-Physical Column Pointer)
1	1	1	Direct to (319-Physical Page Pointer)	Direct to (239-Physical Column Pointer)

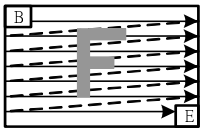
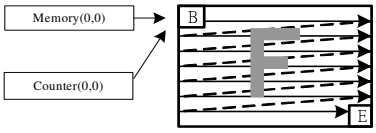
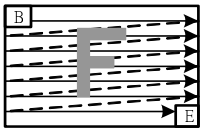
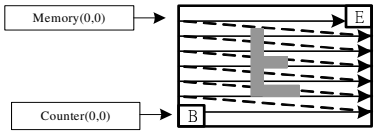
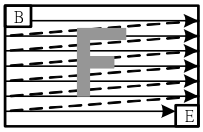
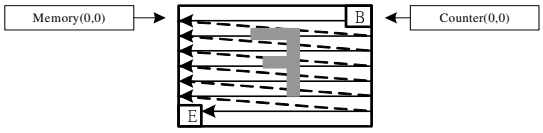
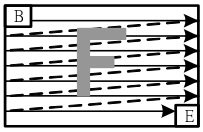
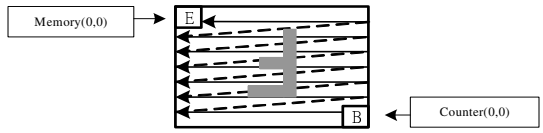
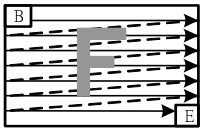
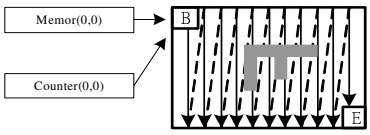
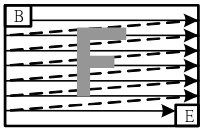
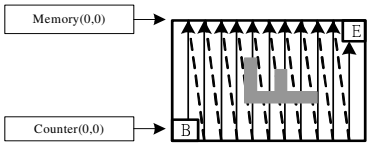
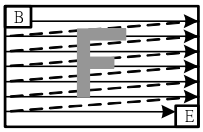
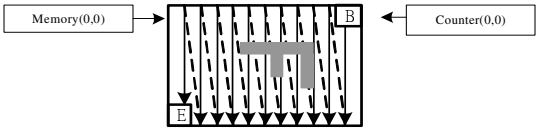
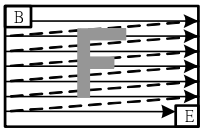
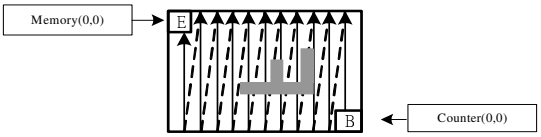
Condition	Column Counter	Page counter
When RAMWR/RAMRD command is accepted	Return to “Start column”	Return to “Start Page”
Complete Pixel Read/Write action	Increment by 1	No change
The Column values is large than “End Column”	Return to “Start column”	Increment by 1
The Page counter is large than “End Page”	Return to “Start column”	Return to “Start Page”

Note:

Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by MADCTL bits B7, B6 and B5. The write order for each pixel unit is

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

One pixel unit represents 1 column and 1 page counter value on the Frame Memory.

Display Data Direction	MADCTR Parameter			Image in the Memory (MPU)	Image in the Driver (Frame Memory)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
XY Exchange X-Mirror	1	1	0		
XY Exchange XY-Mirror	1	1	1		

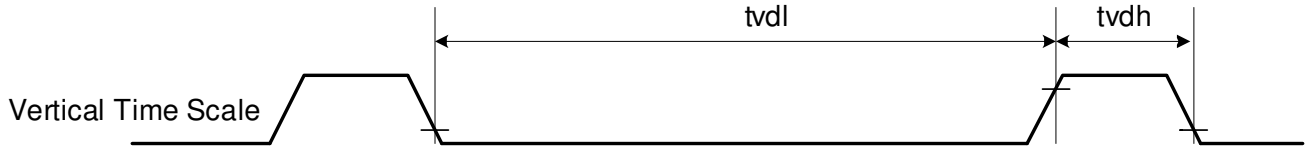
10. Tearing Effect Output

The Tearing Effect output line supplies to the MCU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect Signal is defined by the parameter of the Tearing Effect Line Off & On commands.

The signal can be used by the MCU to synchronize Frame Memory Writing when displaying video images.

10.1. Tearing Effect Line Modes

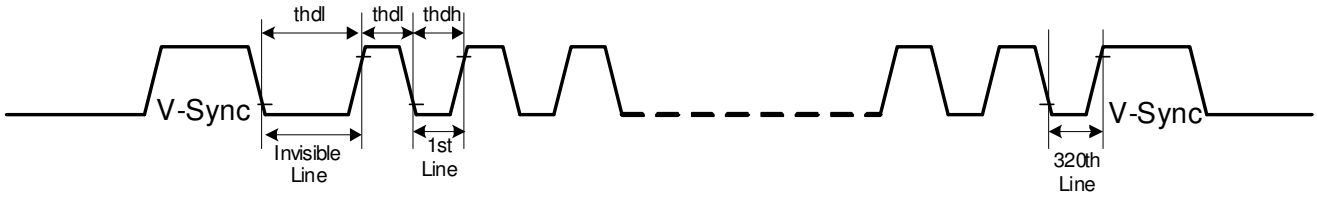
Mode 1, the Tearing Effect Output signal consists of V-Sync information only:



tvdh = The LCD display is not updated from the Frame Memory.

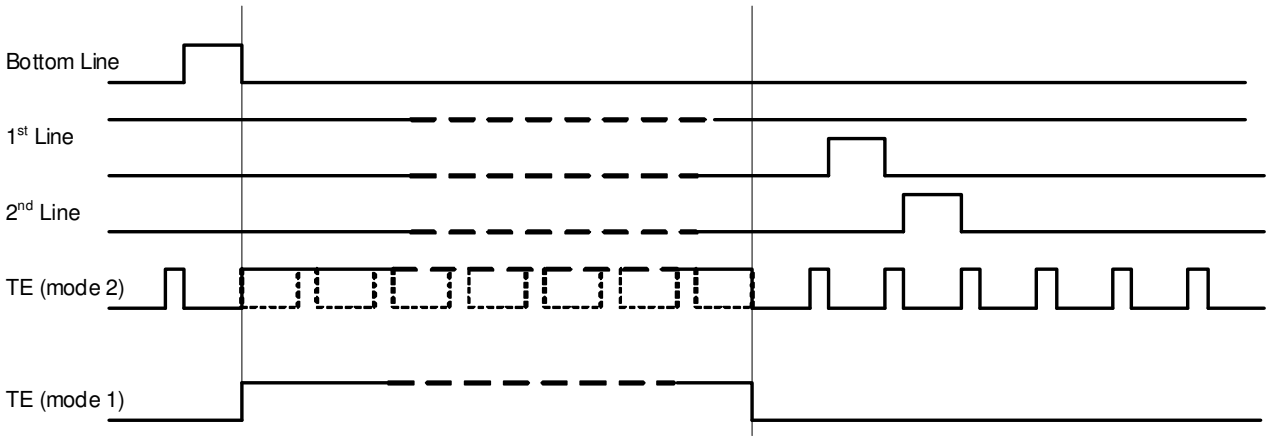
tvdl = The LCD display is updated from the Frame Memory (except Invisible Line – see below).

Mode 2, the tearing effect output signal consists of V-Sync and H-Sync information; there is one V-sync and 320 H-sync pulses per field:



thdh = The LCD display is not updated from the Frame Memory.

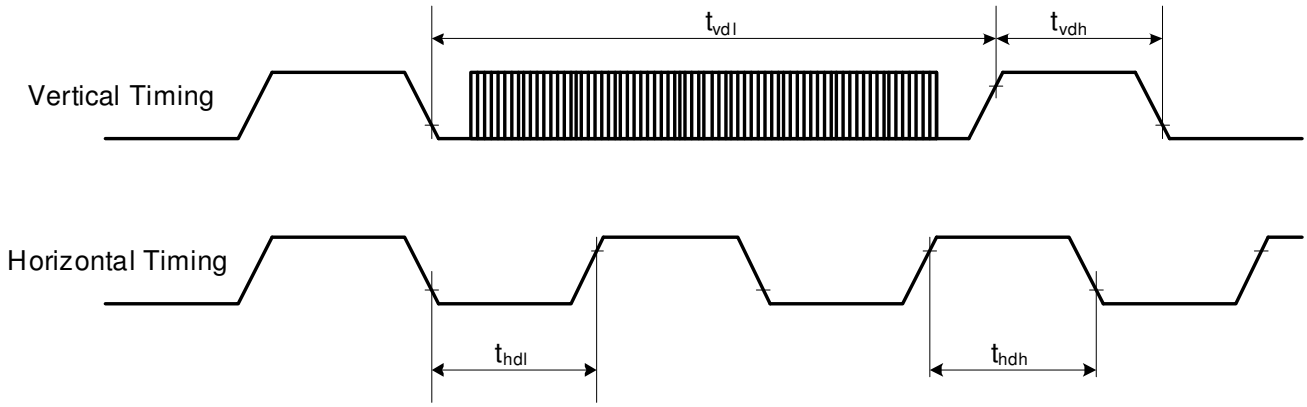
thdl = The LCD display is updated from the Frame Memory (except Invisible Line – see above).



Note: During Sleep In Mode, the Tearing Effect Output Pin is active Low.

10.2. Tearing Effect Line Timings

The tearing effect signal is described below:

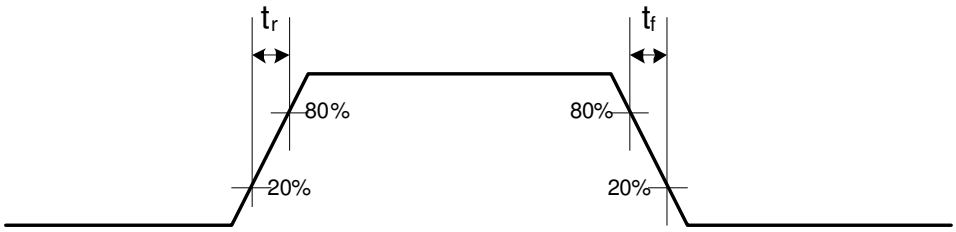


AC characteristics of Tearing Effect Signal (Frame Rate = 60Hz)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Description
t_{vdl}	Vertical timing low duration	--	--	--	ms	
t_{vdh}	Vertical timing high duration	1000	--	--	us	
t_{hdl}	Horizontal timing low duration	--	--	--	us	
t_{hdh}	Horizontal timing high duration	--	--	500	us	

Note:

1. The timings in Table as above apply when MADCTL B4=0 and B4=1
2. The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.



The Tearing Effect Output Line is fed back to the MCU and should be used to avoid Tearing Effect.

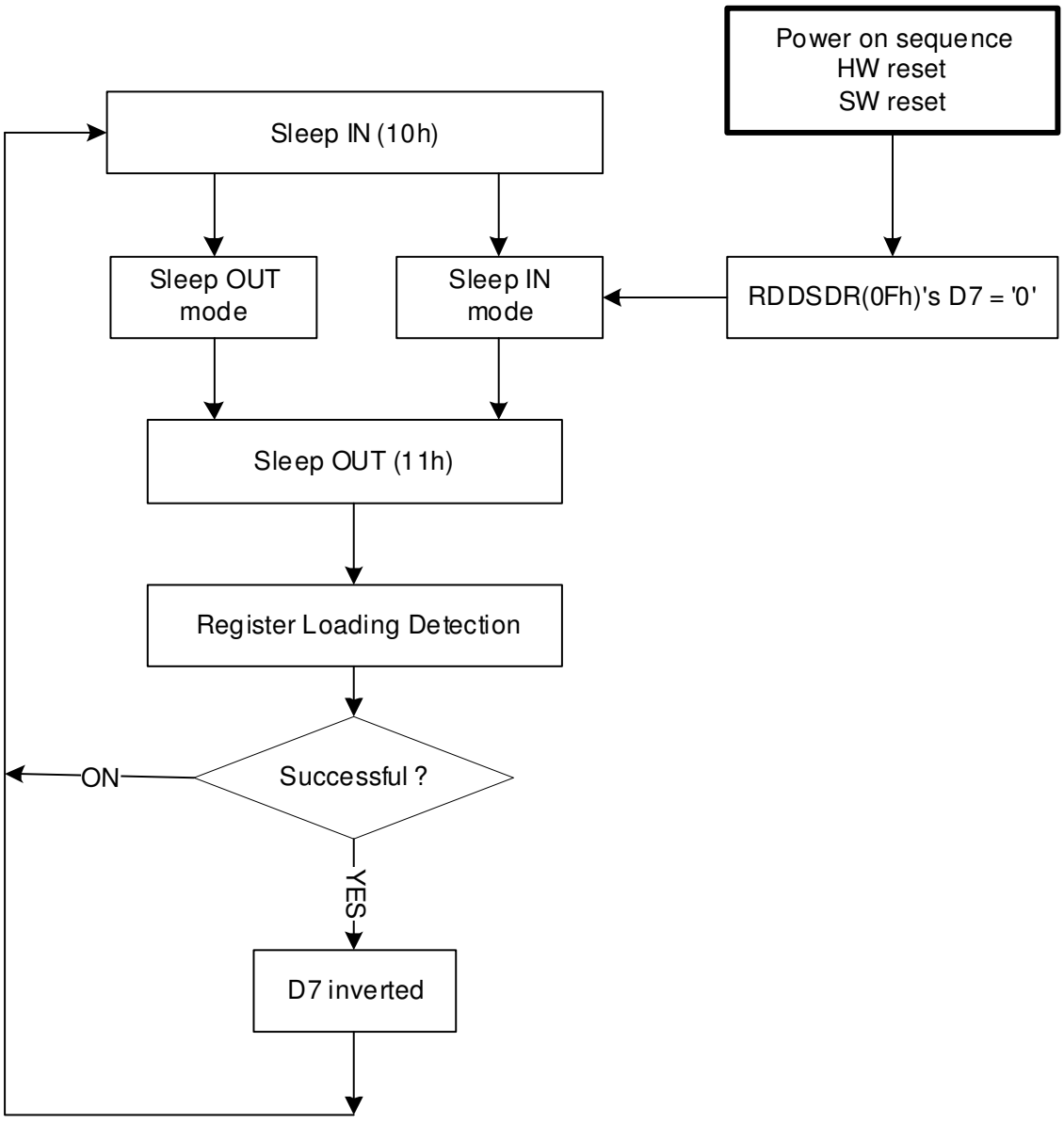
11. Sleep Out – Command and Self-Diagnostic Functions of the Display Module

11.1. Register loading Detection

Sleep Out-command (Command “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from EV Memory(or similar device) to registers of the display controller is working properly.

If the register loading detection is successfully, there is inverted (= increased by 1) a bit, which is defined in command “Read Display Self-Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D7). If it is failure, this bit (D7) is not inverted (= not increased by 1).

The flow chart for this internal function is following:

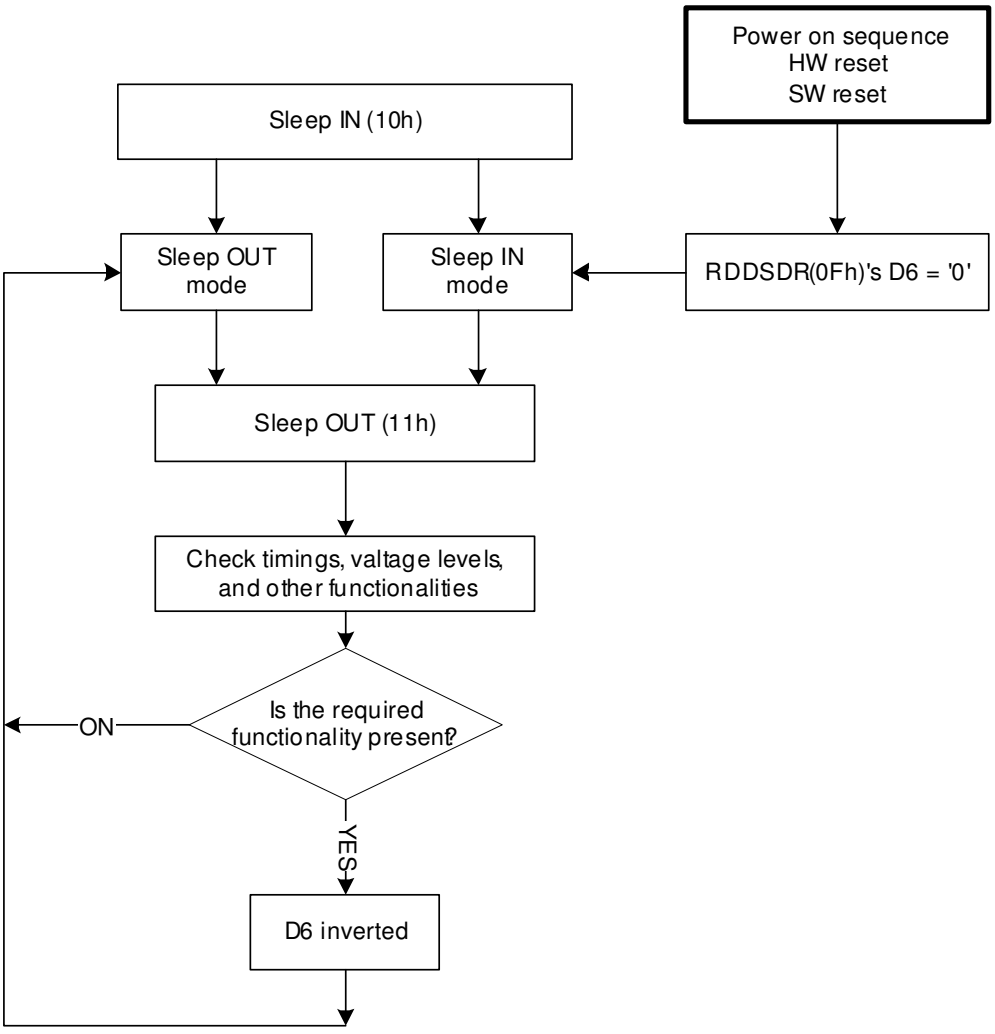


11.2. Functionality Detection

Sleep Out-command (Command “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if the display module is still meeting functionality requirements (e.g. booster voltage levels, timings, etc.) If functionality requirement is met, there is an inverted (= increased by 1) bit, which defined in command “Read Display Self- Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D6). If functionality requirement is not same, this bit (D6) is not inverted (= increased by 1). The flow chart for this internal function is shown as below.

The flow chart for this internal function is following:



Note 1: There is needed 120msec after Sleep Out -command, when there is changing from Sleep In –mode to Sleep Out -mode, before there is possible to check if User’s functionality requirements are met and a value of RDDSDR’s D6 is valid. Otherwise, there is 5msec delay for D6’s value, when Sleep Out –command is sent in Sleep Out -mode.

12. Power ON/OFF Sequence

VDDI and VCI can be applied in any order.

VCI and VDDI can be powered down in any order.

During power off, if LCD is in the Sleep Out mode, VCI and VDDI must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VCI can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

Note 1: There will be no damage to the display module if the power sequences are not met.

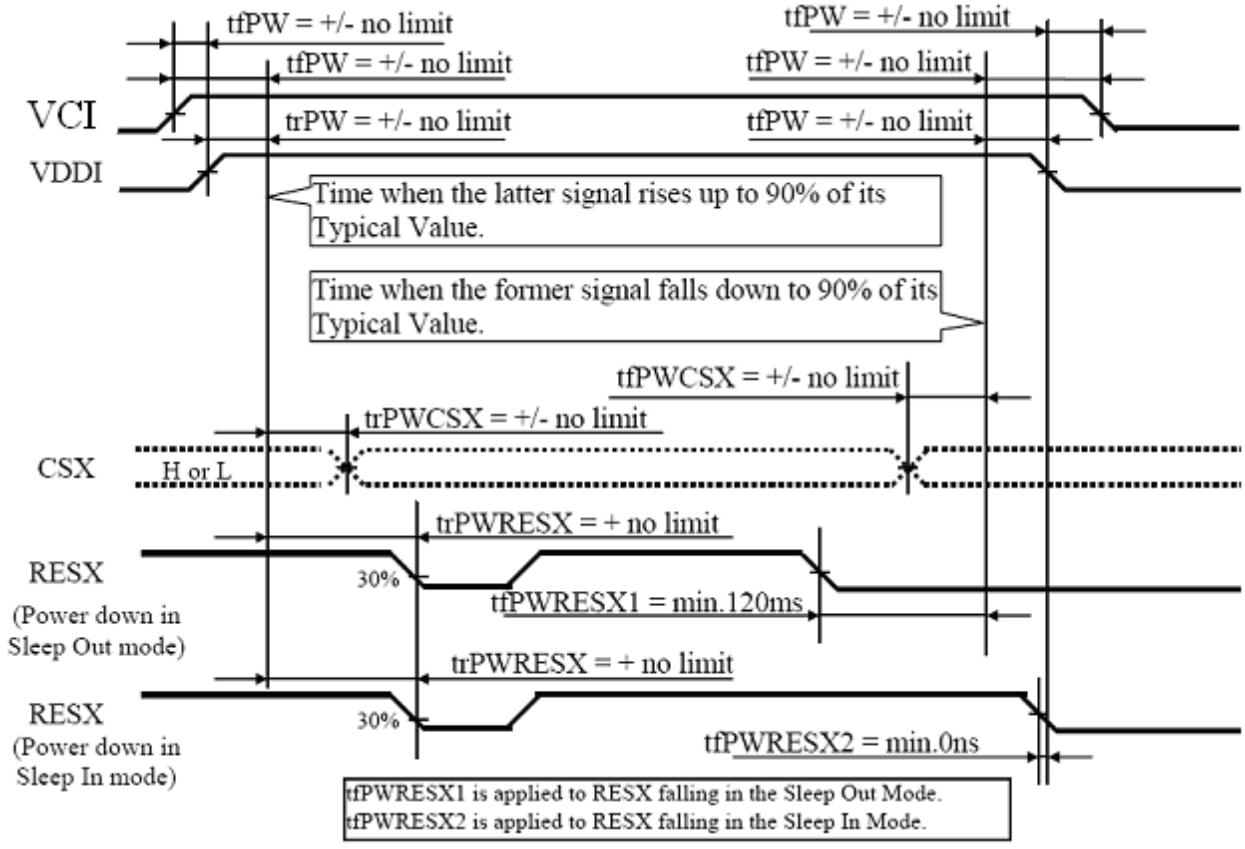
Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.

Note 4: If RESX line is not held stable by host during Power On Sequence as defined in Sections 12.1 and 12.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

12.1. Case 1 – RESX line is held High or Unstable by Host at Power ON

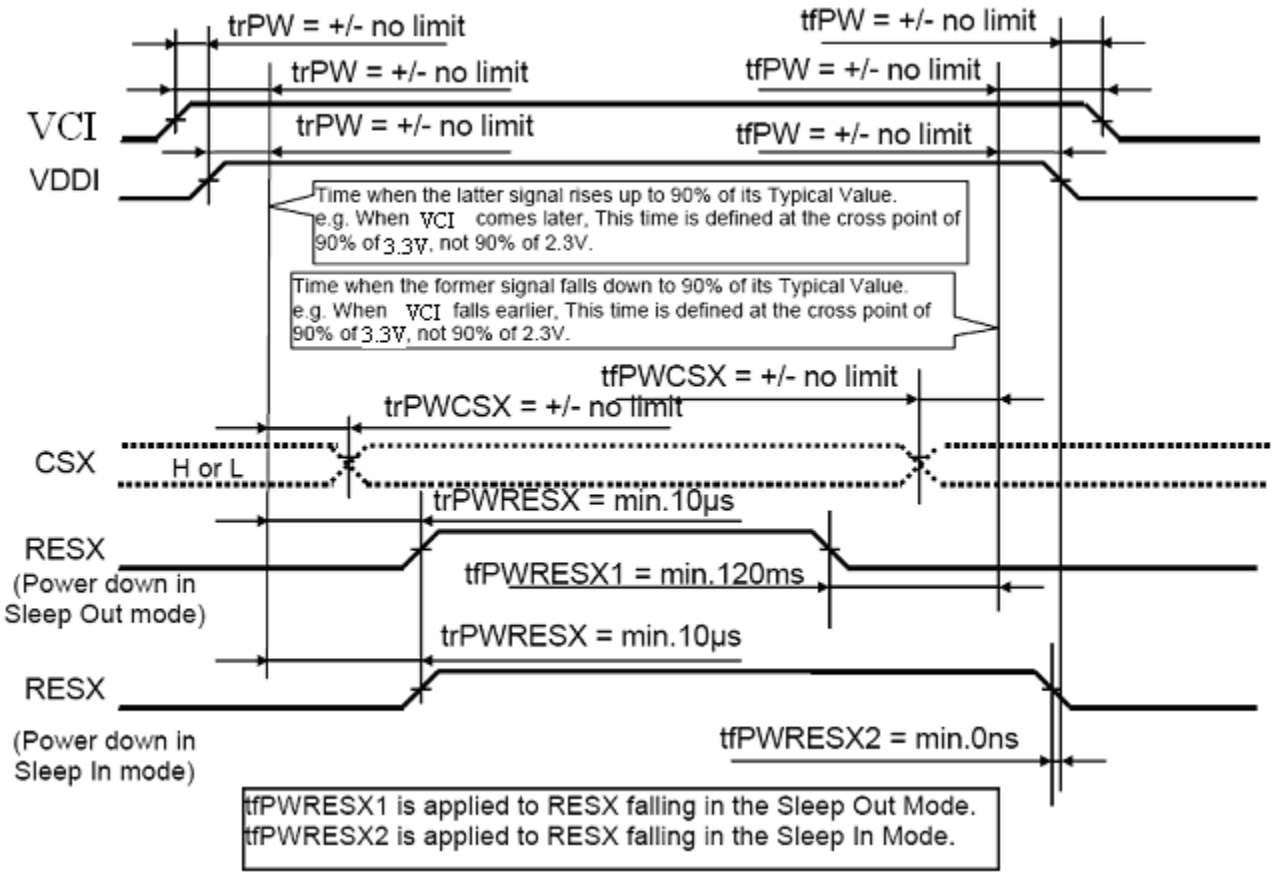
If RESX line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VCI and VDDI have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal power level.

12.2. Case 2 – RESX line is held Low by Host at Power ON

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10µsec after both VCI and VDDI have been applied.



Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal power level.

12.3. Uncontrolled Power Off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an uncontrolled power off event, ILI9340 will force the display to blank and will not be any abnormal visible effects with in 1 second on the display and remains blank until “Power On Sequence” actives.

13. Power Level Definition

13.1. Power Levels

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.

   In this mode, the display is able to show maximum 262,144 colors.

2. Partial Mode On, Idle Mode Off, Sleep Out.

   In this mode part of the display is used with maximum 262,144 colors.

3. Normal Mode On (full display), Idle Mode On, Sleep Out.

   In this mode, the full display area is used but with 8 colors.

4. Partial Mode On, Idle Mode On, Sleep Out.

   In this mode, part of the display is used but with 8 colors.

5. Sleep In Mode.

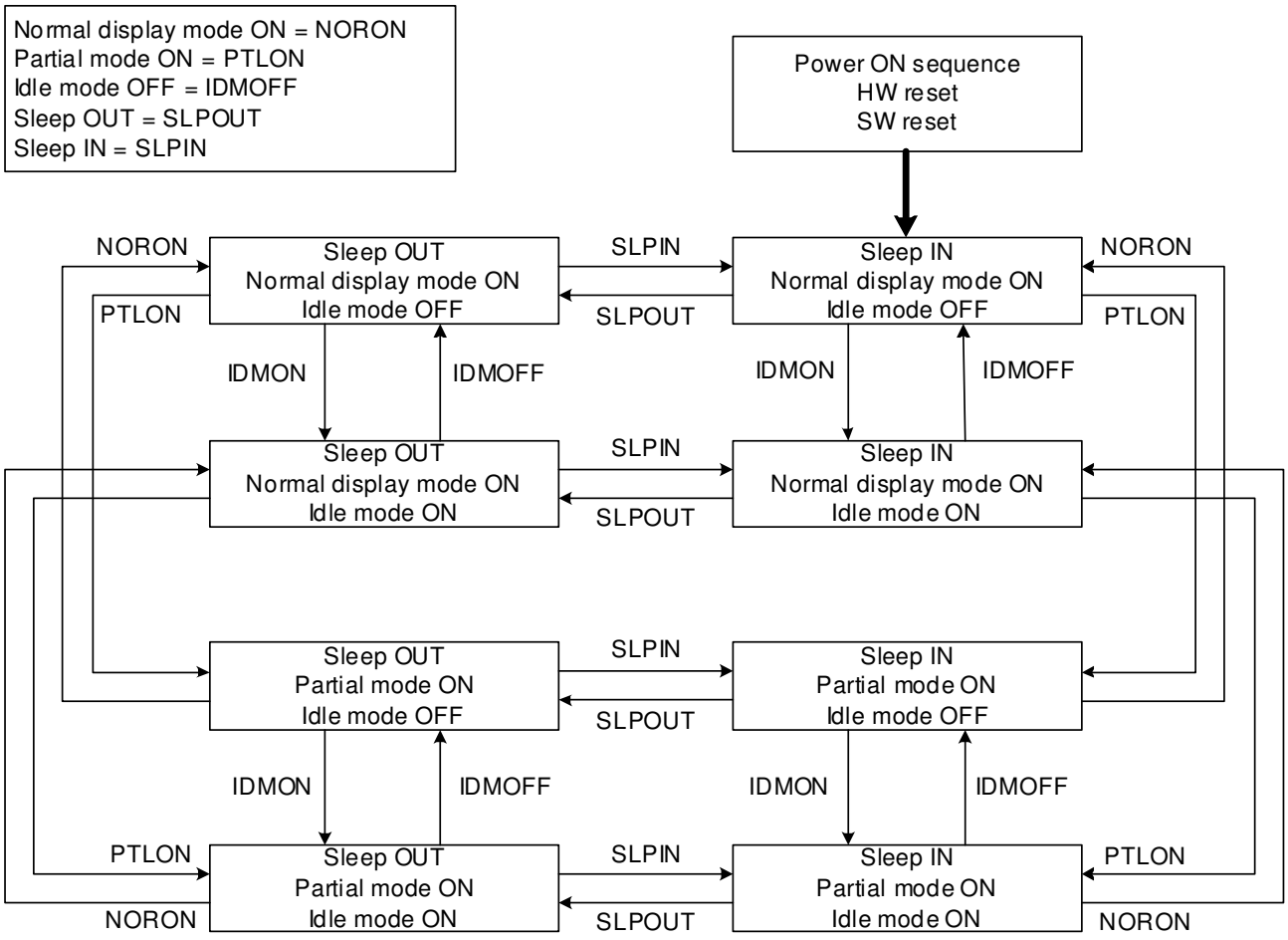
   In this mode, the DC : DC converter, Internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with VDDI and VCI power supply. Contents of the memory are safe.

6. Power Off Mode.

   In this mode, both VCI and VDDI are removed.

Note1: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

13.2. Power Flow Chart

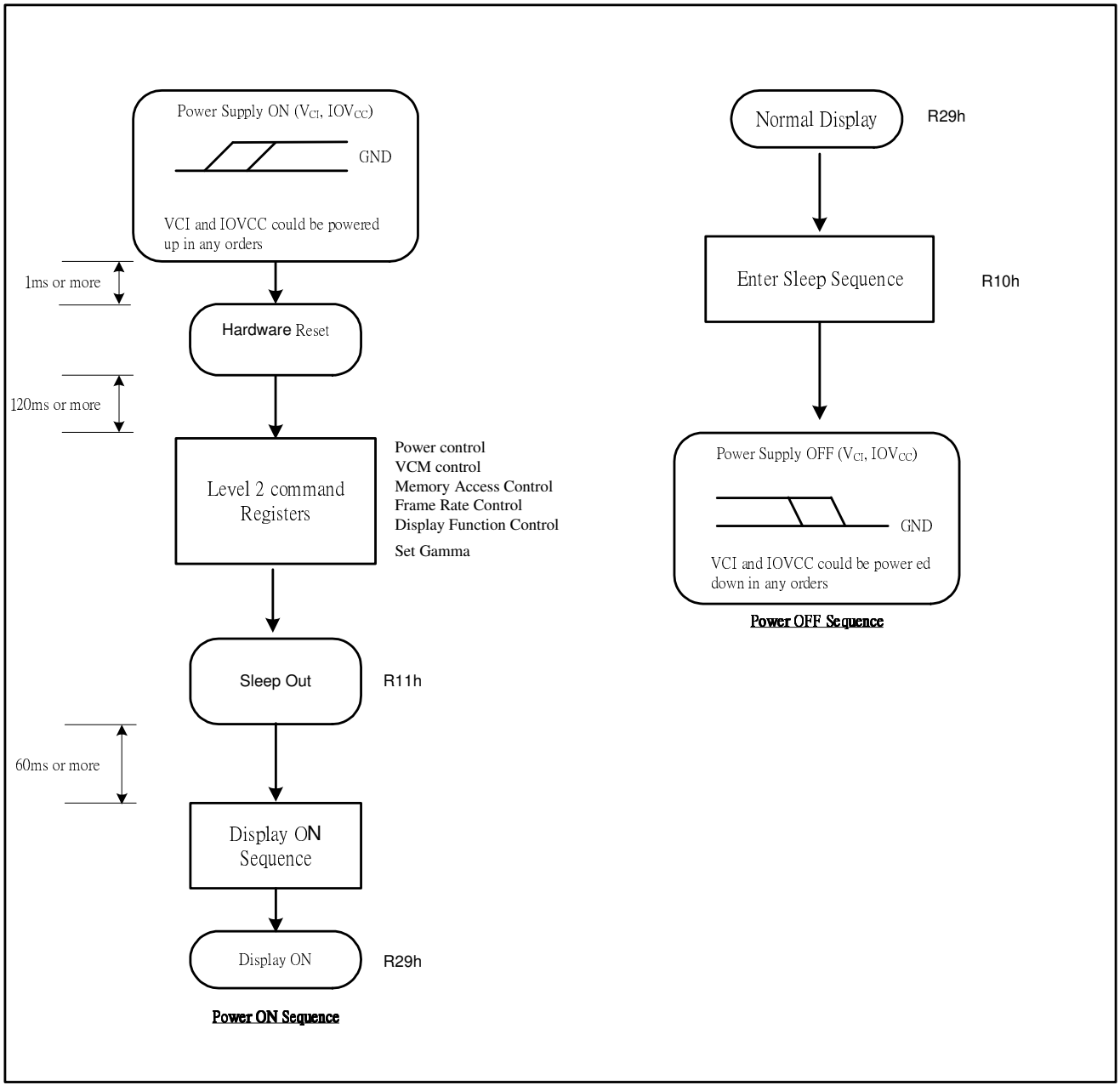


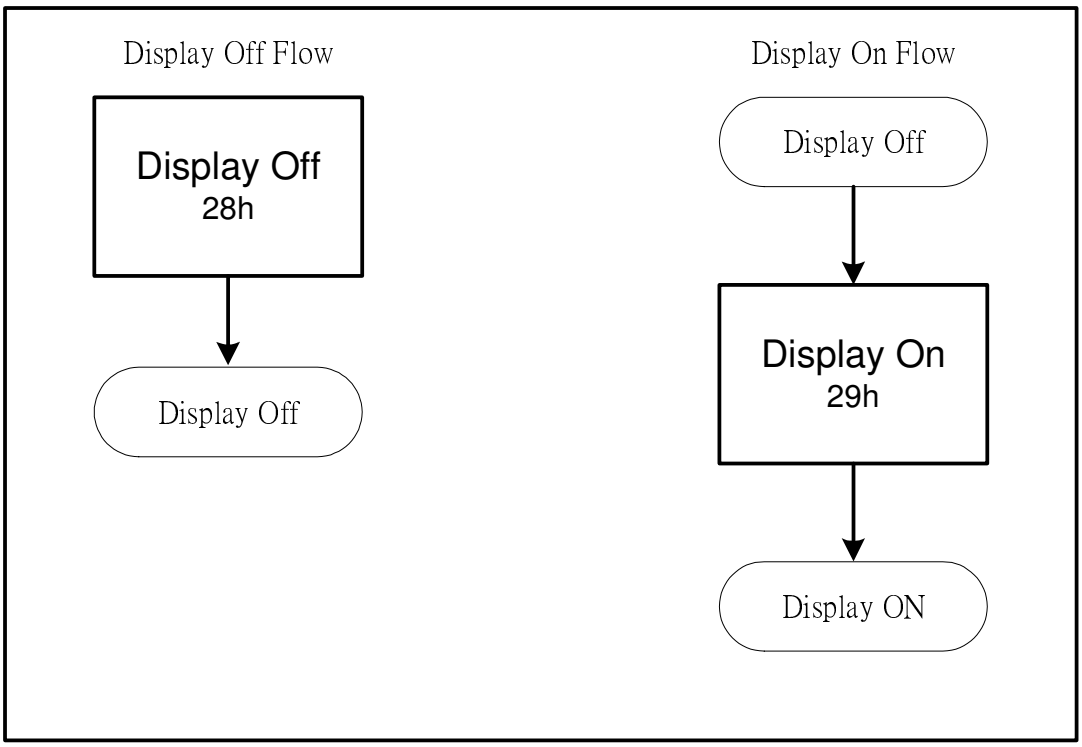
Note 1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.

Note 2: There is not any limitation, which is not specified by User, when there is changing from one power mode to another power mode.

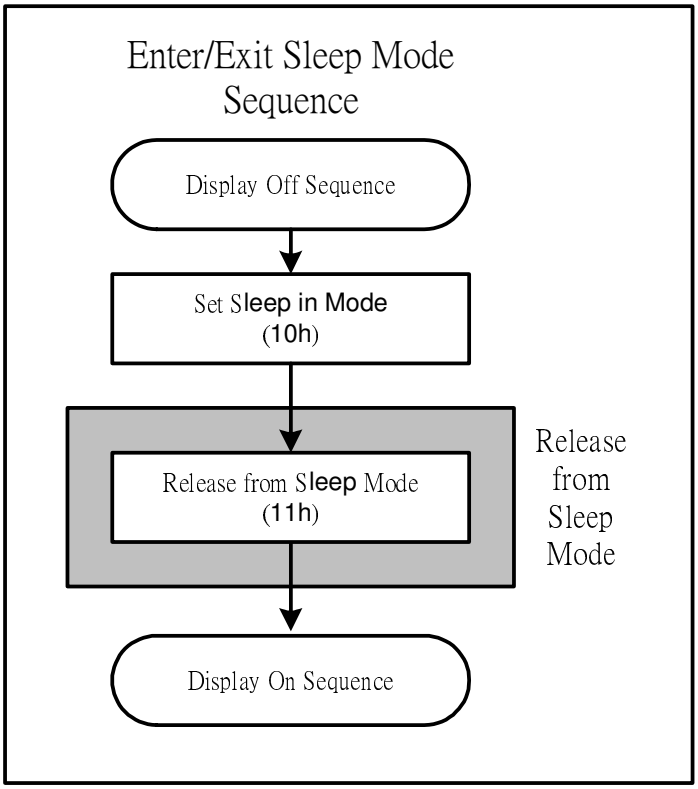
13.3. Power /Display On/Off and Sleep In/Out Sequence

13.3.1. Power /Display On/Off Sequence





13.3.2. Sleep In/Out Sequence



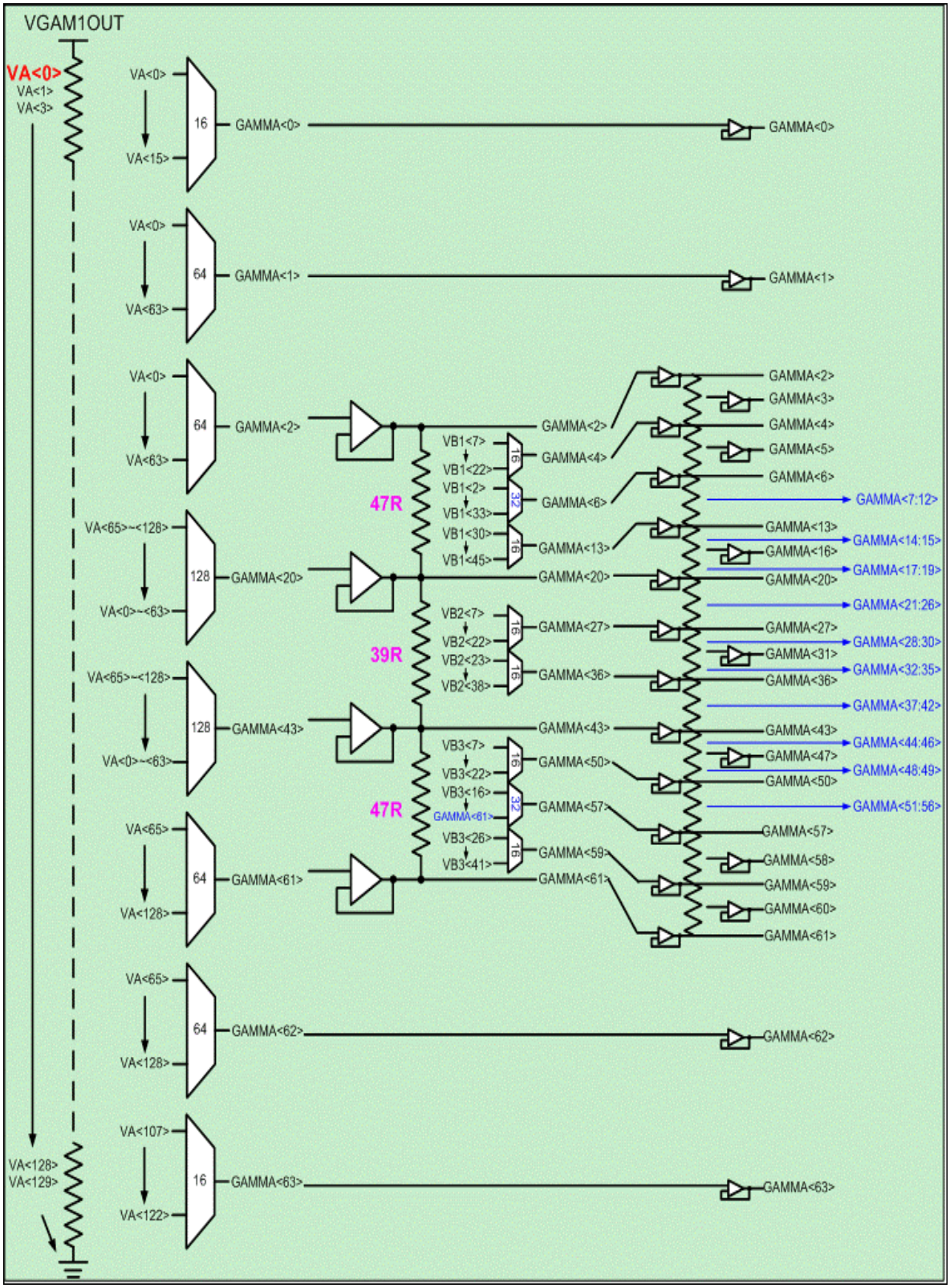
14. Gamma Curves Selection

ILI9340 provide four gamma curves (Gamma1.0, Gamma1.8, Gamma2.2 and Gamma2.5). The gamma curve can be selected by the GC0 to GC3 settings.

14.1. Gamma Default Values (for NW type LC)

Data	Output Voltage									
	VCOM = Low					VCOM = High				
	Gamma	1.0	1.8	2.2	2.5	Gamma	1.0	1.8	2.2	2.5
0	V0P	4.082	4.083	4.084	4.084	V0N	0.279	0.278	0.277	0.276
1	V1P	2.944	3.842	4.015	4.049	V1N	1.278	0.519	0.346	0.310
2	V2P	2.736	3.566	3.843	3.981	V2N	1.623	0.793	0.482	0.345
3	V3P	2.617	3.384	3.681	3.863	V3N	1.728	0.952	0.629	0.465
4	V4P	2.498	3.202	3.518	3.745	V4N	1.834	1.111	0.776	0.585
5	V5P	2.439	3.090	3.445	3.612	V5N	1.891	1.217	0.924	0.736
6	V6P	2.380	2.978	3.371	3.480	V6N	1.948	1.324	1.071	0.887
7	V7P	2.330	2.901	3.285	3.389	V7N	1.995	1.401	1.157	0.980
8	V8P	2.281	2.825	3.199	3.298	V8N	2.042	1.478	1.242	1.073
9	V9P	2.240	2.761	3.128	3.223	V9N	2.081	1.542	1.314	1.150
10	V10P	2.199	2.697	3.056	3.147	V10N	2.120	1.606	1.385	1.228
11	V11P	2.158	2.633	2.985	3.071	V11N	2.159	1.670	1.456	1.305
12	V12P	2.125	2.582	2.928	3.011	V12N	2.191	1.722	1.513	1.367
13	V13P	2.092	2.531	2.871	2.950	V13N	2.222	1.773	1.570	1.429
14	V14P	2.067	2.484	2.802	2.891	V14N	2.249	1.817	1.619	1.484
15	V15P	2.041	2.437	2.733	2.832	V15N	2.276	1.861	1.668	1.540
16	V16P	2.019	2.397	2.674	2.782	V16N	2.299	1.899	1.710	1.587
17	V17P	1.998	2.357	2.615	2.731	V17N	2.322	1.937	1.753	1.634
18	V18P	1.976	2.317	2.557	2.681	V18N	2.345	1.975	1.795	1.682
19	V19P	1.958	2.284	2.508	2.639	V19N	2.365	2.006	1.830	1.721
20	V20P	1.940	2.251	2.458	2.597	V20N	2.384	2.038	1.865	1.761
21	V21P	1.918	2.224	2.425	2.560	V21N	2.404	2.064	1.899	1.798
22	V22P	1.897	2.197	2.391	2.522	V22N	2.424	2.091	1.932	1.836
23	V23P	1.876	2.171	2.357	2.485	V23N	2.444	2.117	1.966	1.873
24	V24P	1.854	2.144	2.323	2.447	V24N	2.464	2.144	2.000	1.911
25	V25P	1.833	2.117	2.289	2.410	V25N	2.484	2.170	2.034	1.948
26	V26P	1.812	2.090	2.256	2.373	V26N	2.504	2.197	2.068	1.986
27	V27P	1.790	2.064	2.222	2.335	V27N	2.524	2.224	2.102	2.023
28	V28P	1.772	2.041	2.193	2.304	V28N	2.540	2.246	2.129	2.052
29	V29P	1.754	2.019	2.165	2.273	V29N	2.557	2.269	2.155	2.082
30	V30P	1.736	1.996	2.136	2.241	V30N	2.574	2.291	2.182	2.111
31	V31P	1.726	1.974	2.108	2.210	V31N	2.591	2.313	2.208	2.141
32	V32P	1.699	1.951	2.080	2.178	V32N	2.609	2.336	2.235	2.170
33	V33P	1.681	1.928	2.051	2.147	V33N	2.625	2.358	2.262	2.199
34	V34P	1.663	1.906	2.023	2.116	V34N	2.642	2.381	2.288	2.229
35	V35P	1.645	1.883	1.994	2.084	V35N	2.659	2.403	2.315	2.258
36	V36P	1.627	1.861	1.966	2.053	V36N	2.676	2.426	2.342	2.287
37	V37P	1.611	1.842	1.942	2.026	V37N	2.694	2.450	2.368	2.317
38	V38P	1.596	1.822	1.917	1.999	V38N	2.713	2.475	2.395	2.346
39	V39P	1.580	1.803	1.893	1.973	V39N	2.731	2.499	2.421	2.376
40	V40P	1.565	1.784	1.869	1.946	V40N	2.749	2.524	2.448	2.405
41	V41P	1.550	1.765	1.845	1.919	V41N	2.768	2.548	2.475	2.434
42	V42P	1.534	1.746	1.820	1.892	V42N	2.786	2.573	2.501	2.464
43	V43P	1.519	1.727	1.796	1.866	V43N	2.805	2.597	2.528	2.493
44	V44P	1.504	1.706	1.776	1.845	V44N	2.819	2.614	2.549	2.513
45	V45P	1.489	1.685	1.755	1.825	V45N	2.834	2.632	2.571	2.533
46	V46P	1.472	1.660	1.730	1.801	V46N	2.852	2.652	2.597	2.557
47	V47P	1.454	1.635	1.706	1.777	V47N	2.869	2.673	2.623	2.581
48	V48P	1.436	1.610	1.681	1.753	V48N	2.887	2.694	2.649	2.605
49	V49P	1.415	1.581	1.653	1.725	V49N	2.908	2.718	2.679	2.633
50	V50P	1.395	1.552	1.624	1.697	V50N	2.928	2.743	2.710	2.661
51	V51P	1.376	1.529	1.598	1.672	V51N	2.947	2.768	2.735	2.688
52	V52P	1.358	1.506	1.573	1.647	V52N	2.966	2.794	2.761	2.715
53	V53P	1.335	1.478	1.541	1.615	V53N	2.990	2.826	2.793	2.749
54	V54P	1.311	1.449	1.508	1.583	V54N	3.013	2.859	2.825	2.783
55	V55P	1.288	1.421	1.476	1.551	V55N	3.037	2.891	2.857	2.817
56	V56P	1.261	1.386	1.438	1.513	V56N	3.065	2.929	2.895	2.858
57	V57P	1.233	1.352	1.400	1.475	V57N	3.093	2.968	2.933	2.899
58	V58P	1.204	1.321	1.359	1.418	V58N	3.145	3.034	2.982	2.955
59	V59P	1.175	1.289	1.319	1.362	V59N	3.196	3.101	3.031	3.011
60	V60P	1.122	1.214	1.246	1.285	V60N	3.243	3.161	3.109	3.081
61	V61P	1.069	1.139	1.173	1.208	V61N	3.290	3.220	3.186	3.151
62	V62P	0.897	1.036	1.070	1.070	V62N	3.428	3.324	3.289	3.255
63	V63P	0.279	0.279	0.279	0.279	V63N	4.083	4.083	4.083	4.083

14.1.1. Grayscale Voltage Generation



14.2. Positive Gamma Correction

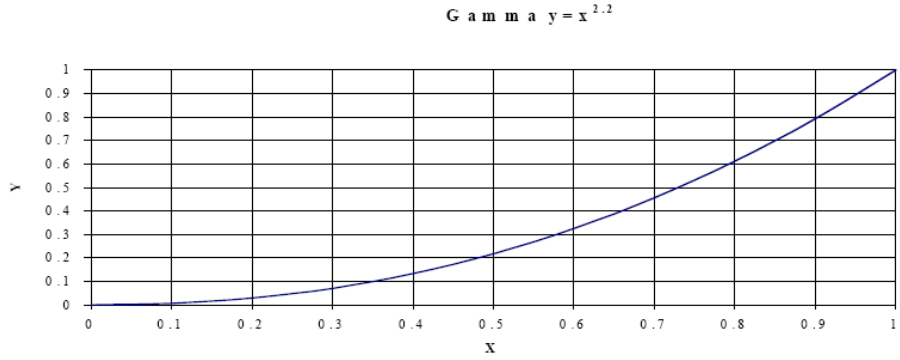
Gamma Level	Value "X" in Formula	Formula	
VP0	VP0[3:0]	(VREG1-VGS)*(130R-X*R)/130R	
VP1	VP1[5:0]	(VREG1-VGS)*(130R-X*R)/130R	
VP2	VP2[5:0]	(VREG1-VGS)*(130R-X*R)/130R	
VP3	—	(VP2-VP4)*35R/(35R*2)+VP4	
VP4	VP4[3:0]	(VP2-VP20)*(47R-X*R-7R)/47R+VP20	
VP5	—	(VP4-VP6)*35R/(35R*2)+VP6	
VP6	VP6[4:0]	(VP2-VP20)*(47R-X*R-2R)/47R+VP20	
VP7	—	(VP6-VP13)*(12R+10R*3+8R*2) /(12R*2+10R*3+8R*2)+VP13	
VP8	—	(VP6-VP13)*(10R*3+8R*2)/(12R*2+10R*3+8R*2)+VP13	
VP9	—	(VP6-VP13)*(10R*2+8R*2)/(12R*2+10R*3+8R*2)+VP13	
VP10	—	(VP6-VP13)*(10R+8R*2)/(12R*2+10R*3+8R*2)+VP13	
VP11	—	(VP6-VP13)*(8R*2)/(12R*2+10R*3+8R*2)+VP13	
VP12	—	(VP6-VP13)*8R/(12R*2+10R*3+8R*2)+VP13	
VP13	VP13[3:0]	(VP2-VP20)*(47R-X*R-30R)/47R+VP20	
VP14	—	(VP13-VP20)*(14R+12R*3+10R*2)/(14R*2+12R*3+10R*2)+VP20	
VP15	—	(VP13-VP20)*(12R*3+10R*2)/(14R*2+12R*3+10R*2)+VP20	
VP16	—	(VP13-VP20)*(12R*2+10R*2)/(14R*2+12R*3+10R*2)+VP20	
VP17	—	(VP13-VP20)*(12R+10R*2)/(14R*2+12R*3+10R*2)+VP20	
VP18	—	(VP13-VP20)*(10R*2)/(14R*2+12R*3+10R*2)+VP20	
VP19	—	(VP13-VP20)*10R/(14R*2+12R*3+10R*2)+VP20	
VP20	VP20[6:0]	<64	(VREG1-VGS)*(130R-X*R)/130R
		>=64	(VREG1-VGS)*(130R-X*R-1R)/130R
VP21	—	(VP20-VP27)*(12R*6)/(12R*7)+VP27	
VP22	—	(VP20-VP27)*(12R*5)/(12R*7)+VP27	
VP23	—	(VP20-VP27)*(12R*4)/(12R*7)+VP27	
VP24	—	(VP20-VP27)*(12R*3)/(12R*7)+VP27	
VP25	—	(VP20-VP27)*(12R*2)/(12R*7)+VP27	
VP26	—	(VP20-VP27)*12R/(12R*7)+VP27	
VP27	VP27[3:0]	(VP20-VP43)*(39R-X*R-7R)/39R+VP43	
VP28	—	(VP27-VP36)*(8R*8)/(8R*9)+VP36	
VP29	—	(VP27-VP36)*(8R*7)/(8R*9)+VP36	
VP30	—	(VP27-VP36)*(8R*6)/(8R*9)+VP36	
VP31	—	(VP27-VP36)*(8R*5)/(8R*9)+VP36	
VP32	—	(VP27-VP36)*(8R*4)/(8R*9)+VP36	
VP33	—	(VP27-VP36)*(8R*3)/(8R*9)+VP36	
VP34	—	(VP27-VP36)*(8R*2)/(8R*9)+VP36	
VP35	—	(VP27-VP36)*8R/(8R*9)+VP36	
VP36	VP36[3:0]	(VP20-VP43)*(39R-X*R-23R)/39R+VP43	
VP37	—	(VP36-VP43)*(12R*6)/(12R*7)+VP43	
VP38	—	(VP36-VP43)*(12R*5)/(12R*7)+VP43	
VP39	—	(VP36-VP43)*(12R*4)/(12R*7)+VP43	
VP40	—	(VP36-VP43)*(12R*3)/(12R*7)+VP43	
VP41	—	(VP36-VP43)*(12R*2)/(12R*7)+VP43	
VP42	—	(VP36-VP43)*12R/(12R*7)+VP43	
VP43	VP43[6:0]	<64	(VREG1-VGS)*(130R-X*R)/130R
		>=64	(VREG1-VGS)*(130R-X*R-1R)/130R
VP44	—	(VP43-VP50)*(14R*2+12R*3+10R)/(14R*2+12R*3+10R*2)+VP50	
VP45	—	(VP43-VP50)*(14R*2+12R*3)/(14R*2+12R*3+10R*2)+VP50	
VP46	—	(VP43-VP50)*(14R*2+12R*2)/(14R*2+12R*3+10R*2)+VP50	
VP47	—	(VP43-VP50)*(14R*2+12R)/(14R*2+12R*3+10R*2)+VP50	
VP48	—	(VP43-VP50)*(14R*2)/(14R*2+12R*3+10R*2)+VP50	
VP49	—	(VP43-VP50)*14R/(14R*2+12R*3+10R*2)+VP50	
VP50	VP50[3:0]	(VP43-VP61)*(47R-X*R-7R)/47R+VP61	
VP51	—	(VP50-VP57)*(12R*2+10R*3+8R)/(12R*2+10R*3+8R*2)+VP57	
VP52	—	(VP50-VP57)*(12R*2+10R*3)/(12R*2+10R*3+8R*2)+VP57	
VP53	—	(VP50-VP57)*(12R*2+10R*2)/(12R*2+10R*3+8R*2)+VP57	
VP54	—	(VP50-VP57)*(12R*2+10R)/(12R*2+10R*3+8R*2)+VP57	
VP55	—	(VP50-VP57)*(12R*2)/(12R*2+10R*3+8R*2)+VP57	
VP56	—	(VP50-VP57)*12R/(12R*2+10R*3+8R*2)+VP57	
VP57	VP57[4:0]	(VP43-VP61)*(47R-X*R-16R)/47R+VP61	
VP58	—	(VP57-VP59)*35R/(35R*2)+VP59	
VP59	VP59[3:0]	(VP43-VP61)*(47R-X*R-26R)/47R+VP61	
VP60	—	(VP59-VP61)*35R/(35R*2)+VP61	
VP61	VP61[5:0]	(VREG1-VGS)*(65R-X*R)/130R	
VP62	VP62[5:0]	(VREG1-VGS)*(65R-X*R)/130R	
VP63	VP63[3:0]	(VREG1-VGS)*(23R-X*R)/130R	

14.3. Negative Gamma Correction

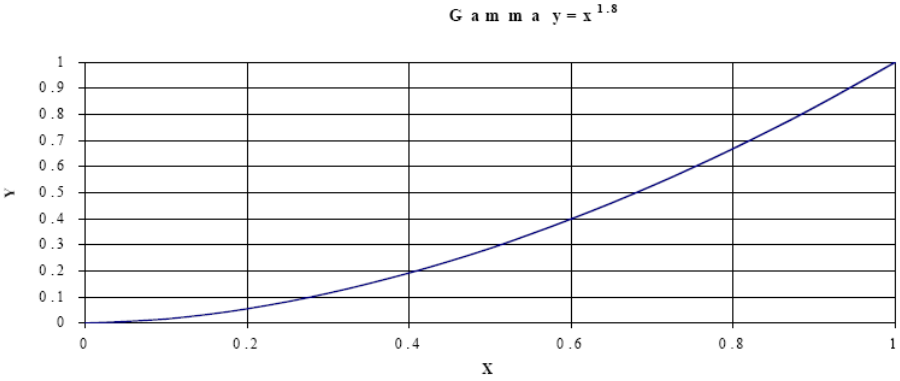
Gamma Level	Value "X" in Formula	Formula	
VN63	VN63[3:0]	(VREG1-VGS)*(130R-X*R)/130R	
VN62	VN62[5:0]	(VREG1-VGS)*(130R-X*R)/130R	
VN61	VN61[5:0]	(VREG1-VGS)*(130R-X*R)/130R	
VN60	—	(VN61-VN59)*35R/(35R*2)+VN59	
VN59	VN59[3:0]	(VN61-VN43)*(47R-X*R-7R)/47R+VN43	
VN58	—	(VN59-VN57)*35R/(35R*2)+VN57	
VN57	VN57[4:0]	(VN61-VN43)*(47R-X*R-2R)/47R+VN43	
VN56	—	(VN57-VN50)*(12R+10R*3+8R*2)/(12R*2+10R*3+8R*2)+VN50	
VN55	—	(VN57-VN50)*(10R*3+8R*2)/(12R*2+10R*3+8R*2)+VN50	
VN54	—	(VN57-VN50)*(10R*2+8R*2)/(12R*2+10R*3+8R*2)+VN50	
VN53	—	(VN57-VN50)*(10R+8R*2)/(12R*2+10R*3+8R*2)+VN50	
VN52	—	(VN57-VN50)*(8R*2)/(12R*2+10R*3+8R*2)+VN50	
VN51	—	(VN57-VN50)*8R/(12R*2+10R*3+8R*2)+VN50	
VN50	VN50[3:0]	(VN61-VN43)*(47R-X*R-30R)/47R+VN43	
VN49	—	(VN50-VN43)*(14R+12R*3+10R*2)/(14R*2+12R*3+10R*2)+VN43	
VN48	—	(VN50-VN43)*(12R*3+10R*2)/(14R*2+12R*3+10R*2)+VN43	
VN47	—	(VN50-VN43)*(12R*2+10R*2)/(14R*2+12R*3+10R*2)+VN43	
VN46	—	(VN50-VN43)*(12R+10R*2)/(14R*2+12R*3+10R*2)+VN43	
VN45	—	(VN50-VN43)*(10R*2)/(14R*2+12R*3+10R*2)+VN43	
VN44	—	(VN50-VN43)*10R/(14R*2+12R*3+10R*2)+VN43	
VN43	VN43[6:0]	<64	(VREG1-VGS)*(130R-X*R)/130R
		>=64	(VREG1-VGS)*(130R-X*R-1R)/130R
VN42	—	(VN43-VN36)*(12R*6)/(12R*7)+VN36	
VN41	—	(VN43-VN36)*(12R*5)/(12R*7)+VN36	
VN40	—	(VN43-VN36)*(12R*4)/(12R*7)+VN36	
VN39	—	(VN43-VN36)*(12R*3)/(12R*7)+VN36	
VN38	—	(VN43-VN36)*(12R*2)/(12R*7)+VN36	
VN37	—	(VN43-VN36)*12R/(12R*7)+VN36	
VN36	VN36[3:0]	(VN43-VN20)*(39R-X*R-7R)/39R+VN20	
VN35	—	(VN36-VN27)*(8R*8)/(8R*9)+VN27	
VN34	—	(VN36-VN27)*(8R*7)/(8R*9)+VN27	
VN33	—	(VN36-VN27)*(8R*6)/(8R*9)+VN27	
VN32	—	(VN36-VN27)*(8R*5)/(8R*9)+VN27	
VN31	—	(VN36-VN27)*(8R*4)/(8R*9)+VN27	
VN30	—	(VN36-VN27)*(8R*3)/(8R*9)+VN27	
VN29	—	(VN36-VN27)*(8R*2)/(8R*9)+VN27	
VN28	—	(VN36-VN27)*8R/(8R*9)+VN27	
VN27	VN27[3:0]	(VN43-VN20)*(39R-X*R-23R)/39R+VN20	
VN26	—	(VN27-VN20)*(12R*6)/(12R*7)+VN20	
VN25	—	(VN27-VN20)*(12R*5)/(12R*7)+VN20	
VN24	—	(VN27-VN20)*(12R*4)/(12R*7)+VN20	
VN23	—	(VN27-VN20)*(12R*3)/(12R*7)+VN20	
VN22	—	(VN27-VN20)*(12R*2)/(12R*7)+VN20	
VN21	—	(VN27-VN20)*12R/(12R*7)+VN20	
VN20	VN20[6:0]	<64	(VREG1-VGS)*(130R-X*R)/130R
		>=64	(VREG1-VGS)*(130R-X*R-1R)/130R
VN19	—	(VN20-VN13)*(14R*2+12R*3+10R)/(14R*2+12R*3+10R*2)+VN13	
VN18	—	(VN20-VN13)*(14R*2+12R*3)/(14R*2+12R*3+10R*2)+VN13	
VN17	—	(VN20-VN13)*(14R*2+12R*2)/(14R*2+12R*3+10R*2)+VN13	
VN16	—	(VN20-VN13)*(14R*2+12R)/(14R*2+12R*3+10R*2)+VN13	
VN15	—	(VN20-VN13)*(14R*2)/(14R*2+12R*3+10R*2)+VN13	
VN14	—	(VN20-VN13)*14R/(14R*2+12R*3+10R*2)+VN13	
VN13	VN13[3:0]	(VN20-VN2)*(47R-X*R-7R)/47R+VN2	
VN12	—	(VN13-VN6)*(12R*2+10R*3+8R)/(12R*2+10R*3+8R*2)+VN6	
VN11	—	(VN13-VN6)*(12R*2+10R*3)/(12R*2+10R*3+8R*2)+VN6	
VN10	—	(VN13-VN6)*(12R*2+10R*2)/(12R*2+10R*3+8R*2)+VN6	
VN9	—	(VN13-VN6)*(12R*2+10R)/(12R*2+10R*3+8R*2)+VN6	
VN8	—	(VN13-VN6)*(12R*2)/(12R*2+10R*3+8R*2)+VN6	
VN7	—	(VN13-VN6)*12R/(12R*2+10R*3+8R*2)+VN6	
VN6	VN6[4:0]	(VN20-VN2)*(47R-X*R-16R)/47R+VN2	
VN5	—	(VN6-VN4)*35R/(35R*2)+VN4	
VN4	VN4[3:0]	(VN20-VN2)*(47R-X*R-26R)/47R+VN2	
VN3	—	(VN4-VN2)*35R/(35R*2)+VN2	
VN2	VN2[5:0]	(VREG1-VGS)*(65R-X*R)/130R	
VN1	VN1[5:0]	(VREG1-VGS)*(65R-X*R)/130R	
VN0	VN0[3:0]	(VREG1-VGS)*(23R-X*R)/130R	

14.4. Positive Gamma Correction

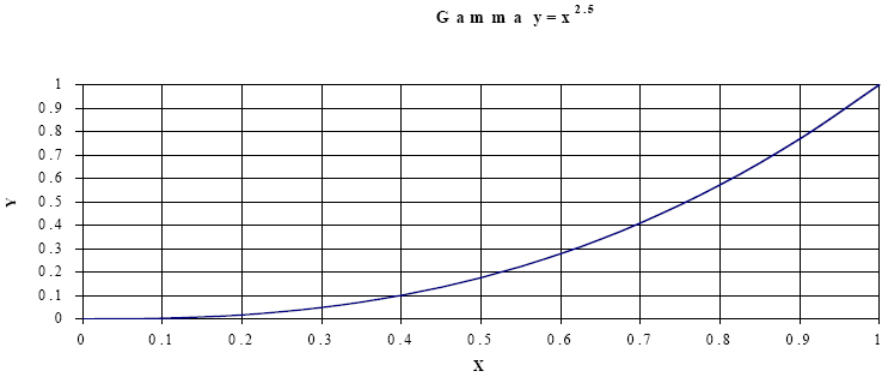
14.4.1. Gamma Curve 1 (GC0), applies the function $y=x^{2.2}$



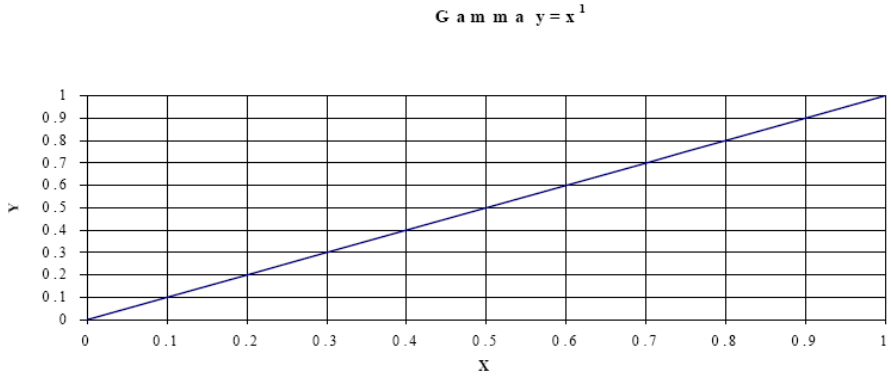
14.4.2. Gamma Curve 2 (GC1), applies the function $y=x^{1.8}$



14.4.3. Gamma Curve 3 (GC2), applies the function $y=x^{2.5}$



14.4.4. Gamma Curve 4 (GC3), applies the function $y=x^{1.0}$



15. Reset

15.1. Registers

The registers that are initialized are listed as below:

	After Powered ON	After Hardware Reset	After Software Reset
Frame Memory	Random	Repair data	No Change
Sleep	In	In	In
Display Mode	Normal	Normal	Normal
Display	Off	Off	Off
Idle	Off	Off	Off
Column Start Address	0000 h	0000 h	0000 h
Column End Address	00EF h	00EF h	If MADCTL's B5=0:00EF h If MADCTL's B5=1:013F h
Page Start Address	0000 h	0000 h	0000 h
Page End Address	013F h	013F h	If MADCTL's B5 = 0:013F h If MADCTL's B5=1:00EF h
Gamma Setting	GC0	GC0	GC0
Partial Area Start	0000 h	0000 h	0000 h
Partial Area End	013F h	013F h	013F h
Memory Data Access Control	00 h	00 h	No Change
RDDPM	08 h	08 h	08 h
RDDMADCTL	00 h	00 h	No Change
RDDCOLMOD	06 h	06 h	06 h
RDDIM	00 h	00 h	00 h
RDDSM	00 h	00 h	00 h
RDDSDR	00 h	00 h	00 h
TE Output Line	Off	Off	Off
TE Line Mode	Mode 1 (Note 3)	Mode 1 (Note 3)	Mode 1 (Note 3)

Note 1: There will be no abnormal visible effects on the display when S/W or H/W Resets are applied.

Note 2: After Powered-On Reset finishes within 10µs after both VCI *& VDDI are applied.*

Note 3: Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.

15.2. Output Pins, I/O Pins

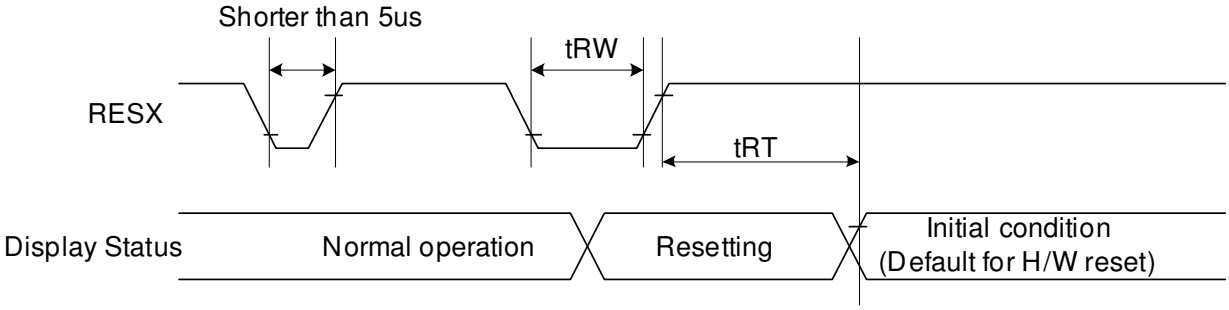
	After Power ON	After Hardware Reset	After Software Reset
TE line	Low	Low	Low
D[17:0] (output driver)	Hi-Z (Inactive)	Hi-Z (Inactive)	Hi-Z (Inactive)

Note 1: There will be no output from D [17:0] during Power ON/OFF sequence, hardware reset and software reset.

15.3. Input Pins

	During Power ON Process	After Power ON	After Hardware Reset	After Software Reset	During Power OFF Process
RESX	See Chapter 12	Input valid	Input valid	Input valid	See Chapter 12
CSX	Input invalid	Input valid	Input valid	Input valid	Input invalid
D/CX	Input invalid	Input valid	Input valid	Input valid	Input invalid
WRX	Input invalid	Input valid	Input valid	Input valid	Input invalid
RDX	Input invalid	Input valid	Input valid	Input valid	Input invalid
D[17:0] (input driver)	Input invalid	Input valid	Input valid	Input valid	Input invalid

15.4. Reset Timing



Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

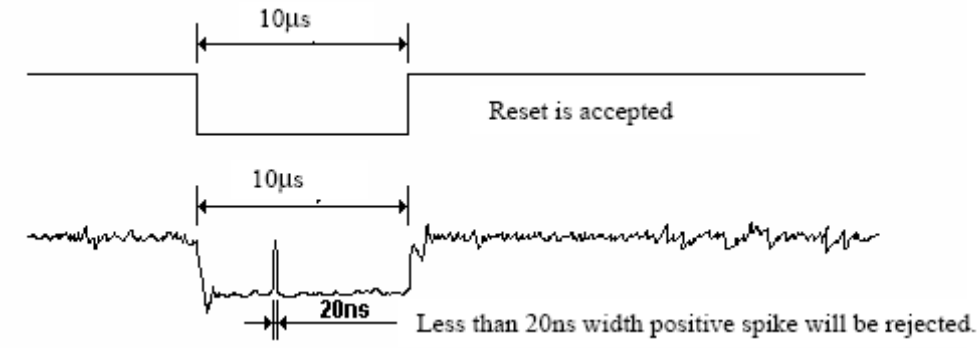
Note 1: The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NV memory to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

Note 2: Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below: -

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

Note 3: During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In -mode.) And then return to Default condition for Hardware Reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:



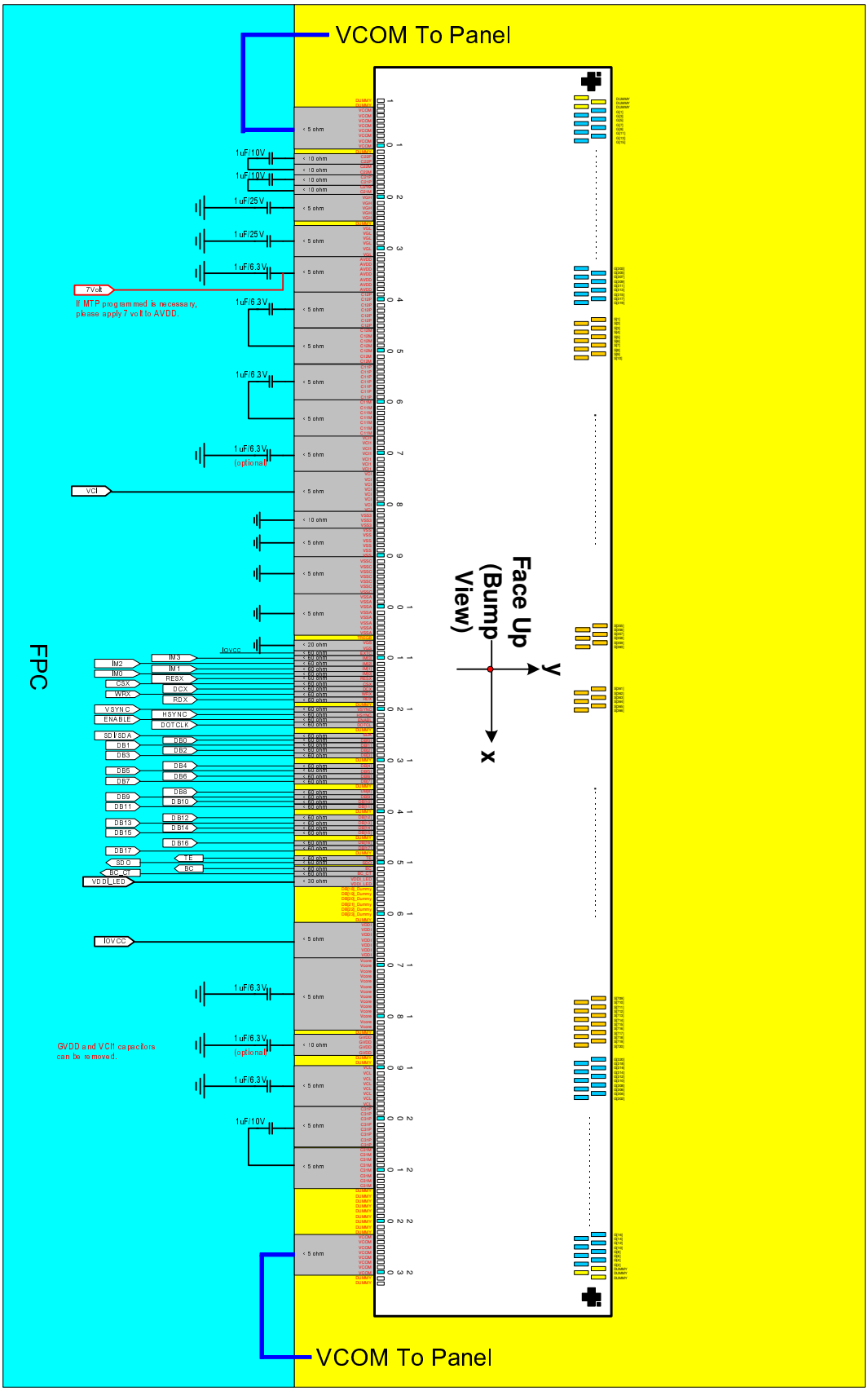
Note 5: When Reset applied during Sleep In Mode.

Note 6: When Reset applied during Sleep Out Mode.

Note 7: It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

16. Application

16.1. Configuration of Power Supply Circuit

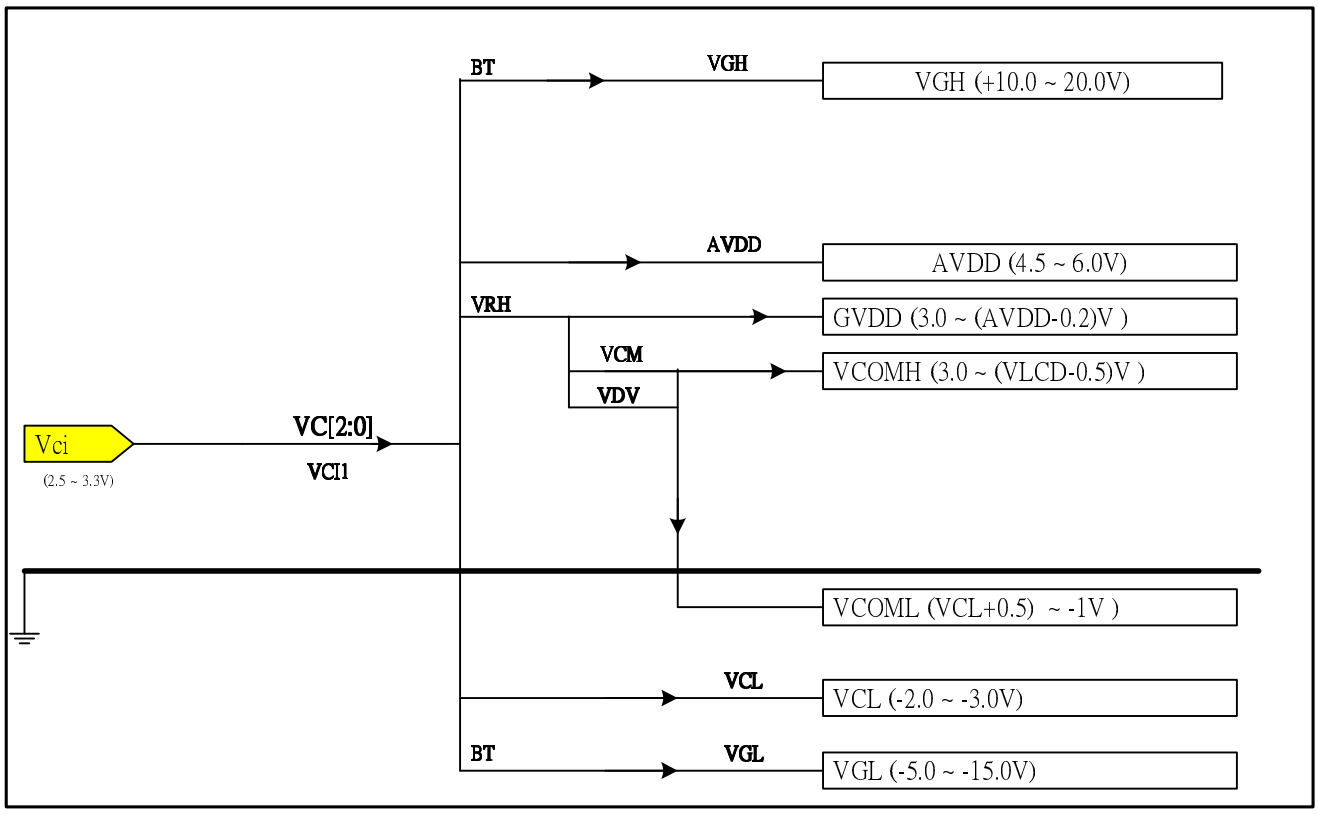


The Following tables shows specifications of external elements connected to the ILI9340's power supply circuit.

Items	Recommended Specification	Pin connection
Capacity 1 F (B characteristics)	6.3V	AVDD, VCORE,VCL,C11P/M, C12P/M, C31P/M
	10V	C21P/M, C22P/M
	25V	VGH, VGL

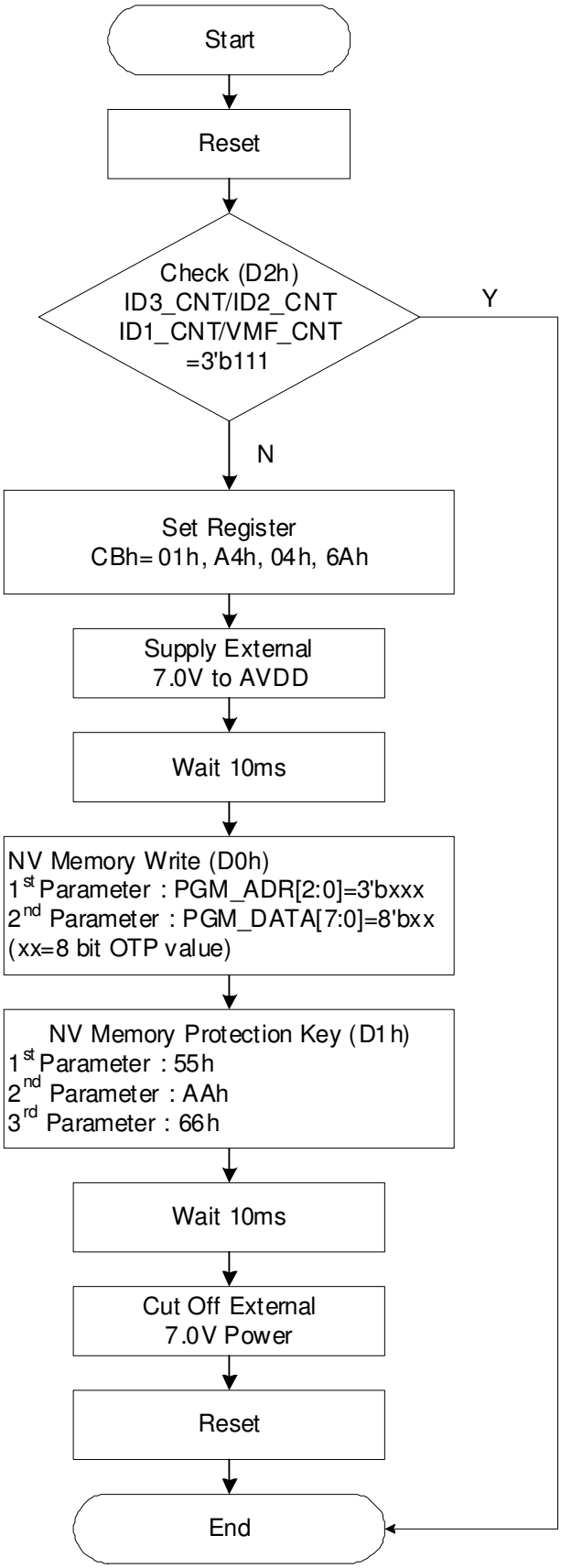
16.2. Voltage Generation

The pattern diagram for setting the voltages and the waveforms of the voltages of the ILI9340 are as follows.



Note: The AVDD, VGH, VGL, and VCL output voltage levels are lower than their theoretical levels (ideal voltage levels) due to current consumption at respective outputs. The voltage levels in the following relationships (AVDD – GVDD) > 0.2V and (VCOML – VCL) > 0.5V are the actual voltage levels. When the alternating cycles of VCOM are set high (e.g. the polarity inverts every line cycle), current consumption is large. In this case, check the voltage before use.

17. NV Memory Programming Flow



18. Electrical Characteristics

18.1. Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When ILI9340 is used out of the absolute maximum ratings, ILI9340 may be permanently damaged. To use ILI9340 within the following electrical characteristics limitation is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, ILI9340 will malfunction and cause poor reliability.

Item	Symbol	Unit	Value
Supply voltage	VCI	V	-0.3 ~ +4.6
Supply voltage (Logic)	VDDI	V	-0.3 ~ +4.6
Supply voltage (Digital)	VCORE	V	-0.3 ~ +2.4
Driver supply voltage	VGH-VGL	V	-0.3 ~ +32.0
Logic input voltage range	VIN	V	-0.3 ~ VDDI + 0.3
Logic output voltage range	VO	V	-0.3 ~ VDDI + 0.3
Operating temperature	Topr	℃	-40 ~ +80
Storage temperature	Tstg	℃	-55 ~ +110
Note: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.			

18.2. DC Characteristics

18.2.1. General DC Characteristics

Item	Symbol	Unit	Condition	Min.	Typ.	Max.	Note
Power and Operation Voltage							
Analog Operating Voltage	VCI	V	Operating voltage	2.5	2.8	3.3	Note2
Logic Operating Voltage	VDDI	V	I/O supply voltage	1.65	2.8	3.3	Note2
Digital Operating voltage	VCORE	V	Digital supply voltage	-	1.8	-	Note2
Gate Driver High Voltage	VGH	V	-	10.0	-	16.0	Note3
Gate Driver Low Voltage	VGL	V	-	-16.0	-	-9.0	Note3
Driver Supply Voltage	-	V	|VGH-VGL|	19	-	32	Note3
Input and Output							
Logic High Level Input Voltage	VIH	V	-	0.8*VDDI	-	VDDI	Note1,2,3
Logic Low Level Input Voltage	VIL	V	-	VSS	-	0.2*VDDI	Note1,2,3
Logic High Level Output Voltage	VOH	V	IOL=-1.0mA	0.8*VDDI	-	VDDI	Note1,2,3
Logic Low Level Output Voltage	VOL	V	IOL=1.0mA	VSS	-	0.2*VDDI	Note1,2,3
Logic Input Leakage Current	ILEA	uA	VIN=VDDI or VSS	-0.1	-	+0.1	Note1,2,3
Current consumption during STB operation	IST	uA	VCC=VCI=IOVCC=2.8V, Ta=25℃, CPU interface		20uA	100uA	Note1,2,3

(VCC, VCI, IOVCC)							
VCOM Operation							
VCOM High Voltage	VCOMH	V	Ccom=12nF	2.5	-	5.0	Note3
VCOM Low Voltage	VCOML	V	Ccom=12nF	-2.5	-	0.0	Note3
VCOM Amplitude Voltage	VCOMA	V	|VCOMH-VCOML|	4.0	-	5.5	Note3
Source Driver							
Source Output Range	Vsout	V	-	0.1	-	AVDD-0.1	Note4
Gamma Reference Voltage	GVDD	V	-	3.0	-	5.0	Note3

Note 1: VDDI=1.65 to 3.3V, VCI=2.5 to 3.3V, AGND=VSS=0V, Ta=-30 to 70 (to +80 no damage) ℃.

Note2: Please supply digital VDDI voltage equal or less than analog VCI voltage.

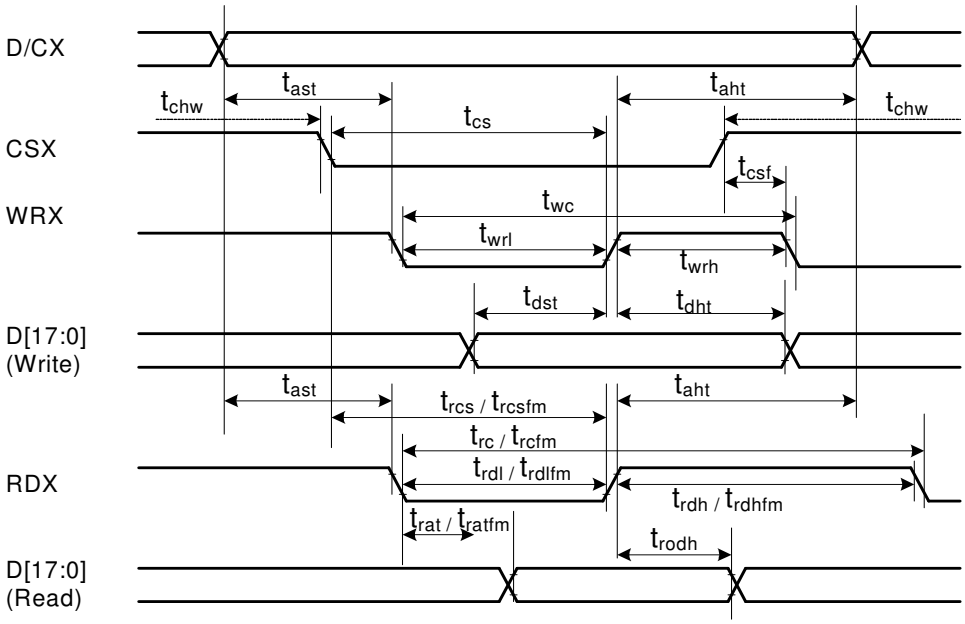
Note3: CSX, RDX, WRX, D[17:0], D/CX, RESX, TE, DOTCLK, VSYNC, HSYNC, DE, SDA, SCL, IM3, IM2, IM1, IM0, and Test pins.

Note4: When the measurements are performed with LCD module. Measurement Points are like Note3.

Note5: Source channel loading = 10pF/channel, Gate channel loading = 50pF/channel

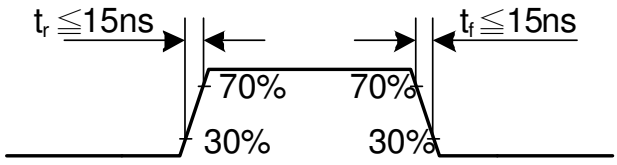
18.3. AC Characteristics

18.3.1. Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080- Ⅰ system)

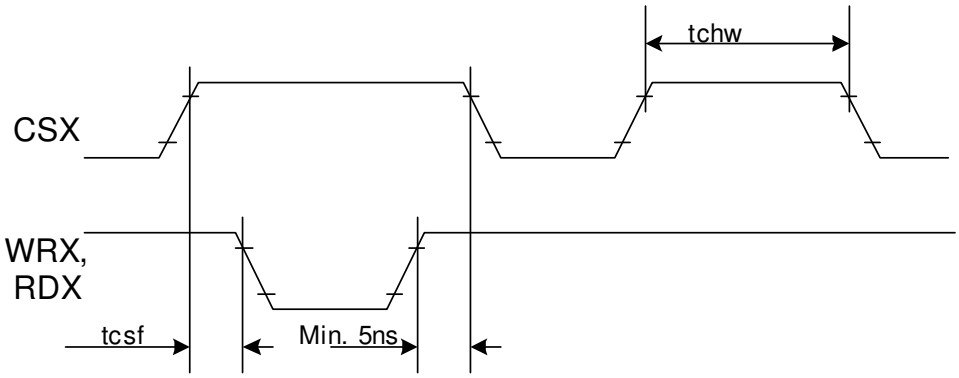


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Write/Read)	10	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	66	-	ns	
	twrh	Write Control pulse H duration	33	-	ns	
	twrl	Write Control pulse L duration	33	-	ns	
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[17:0], D[15:0], D[8:0], D[7:0]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	60	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Note: Ta = -30 to 70 ℃, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V

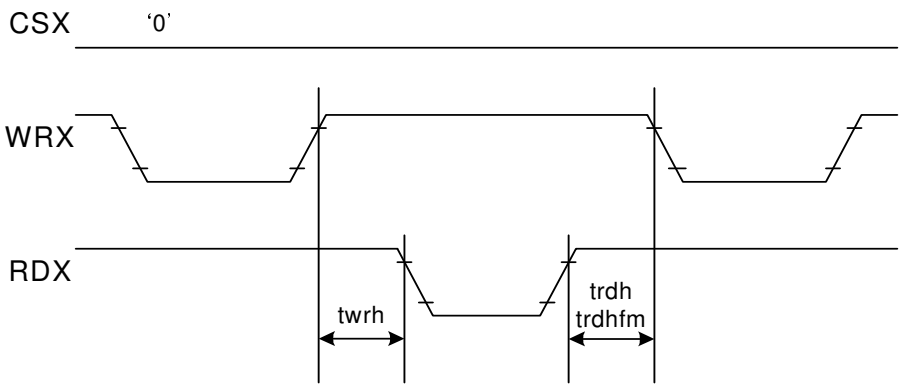


CSX timings :



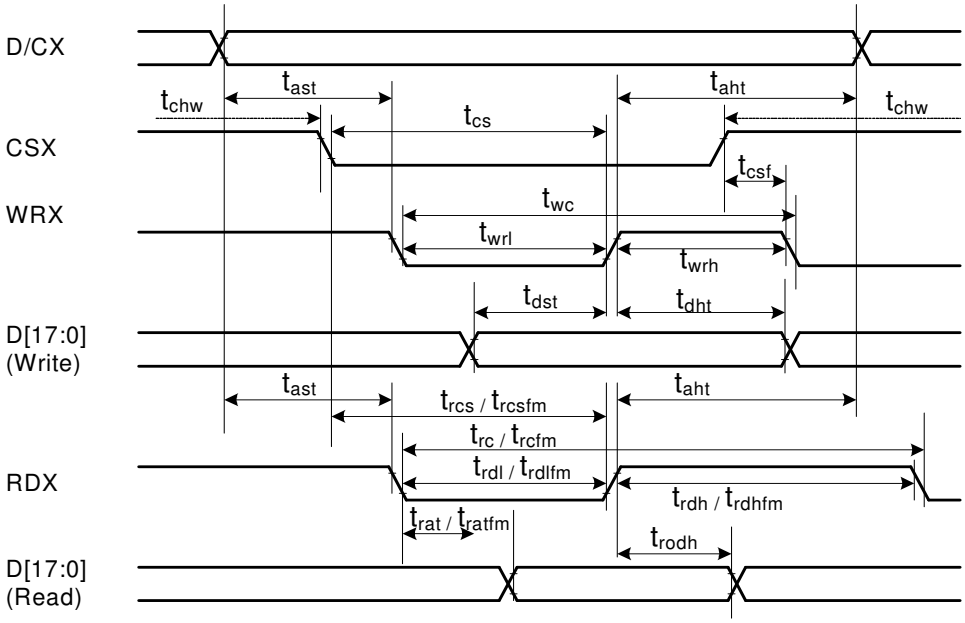
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Write to read or read to write timings:



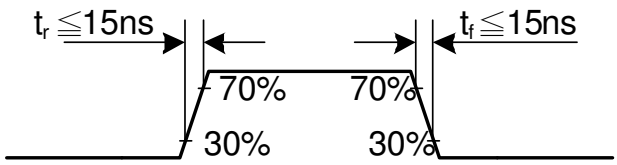
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

18.3.2. Display Parallel 18/16/9/8-bit Interface Timing Characteristics(8080-Ⅱ system)

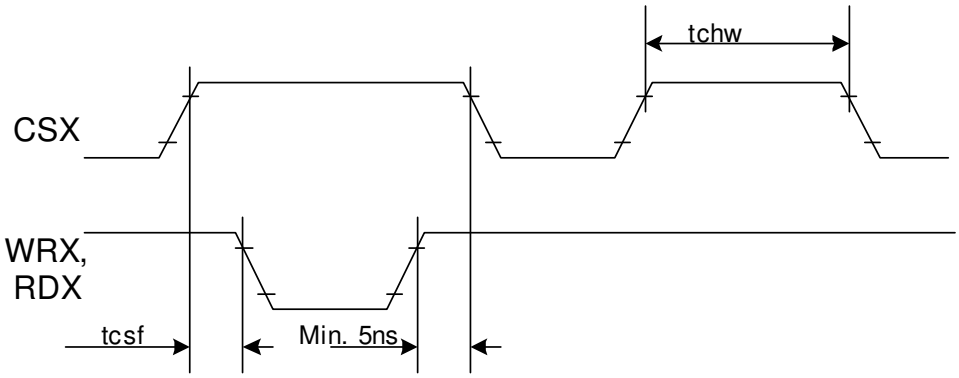


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Write/Read)	10	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	66	-	ns	
	twrh	Write Control pulse H duration	33	-	ns	
	twrl	Write Control pulse L duration	33	-	ns	
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[17:0], D[17:10]&D[8:1], D[17:10], D[17:9]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	60	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Note: Ta = -30 to 70 ℃, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V.

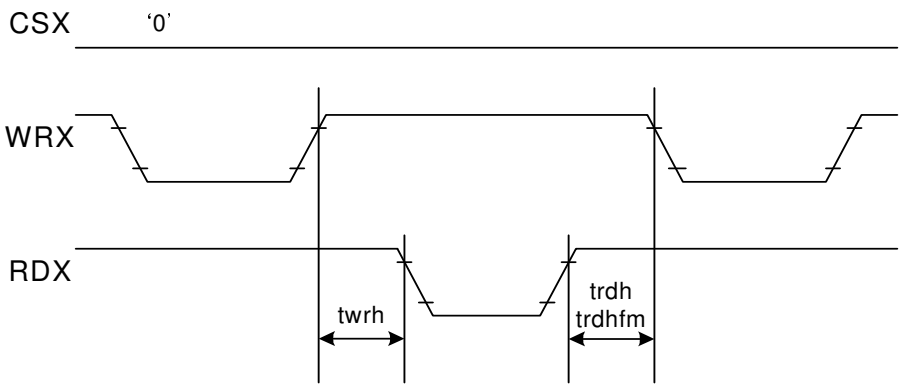


CSX timings :



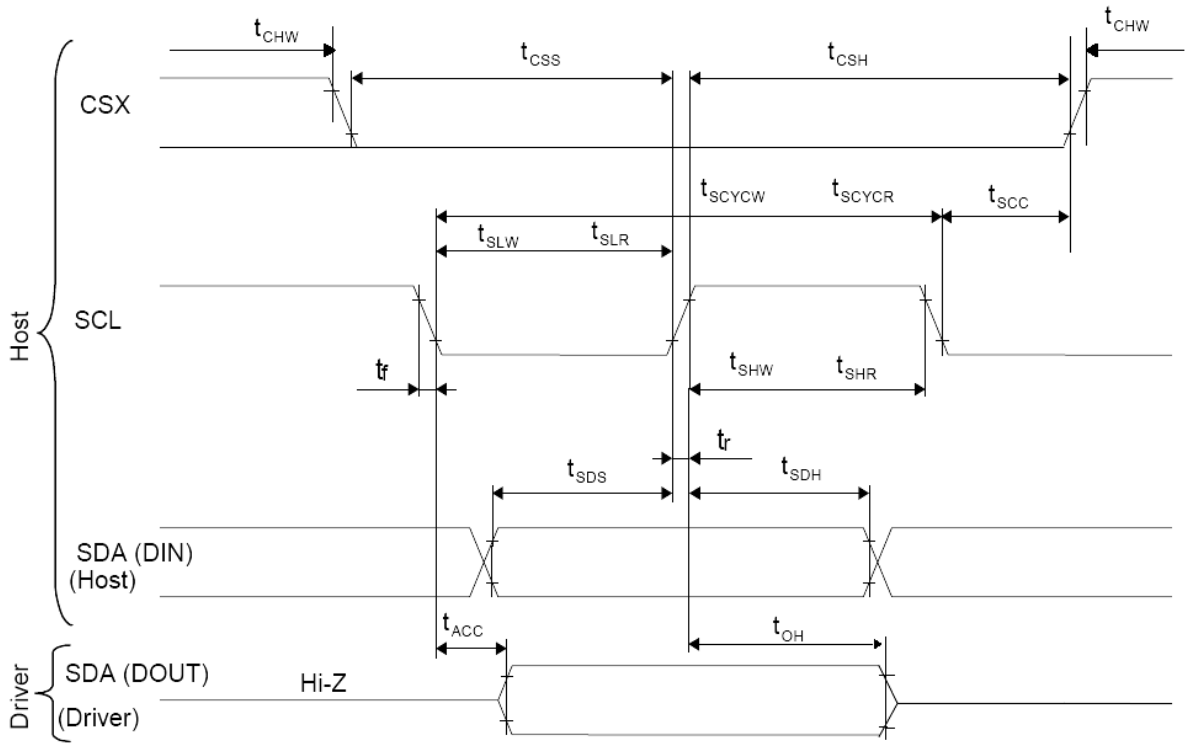
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Write to read or read to write timings:



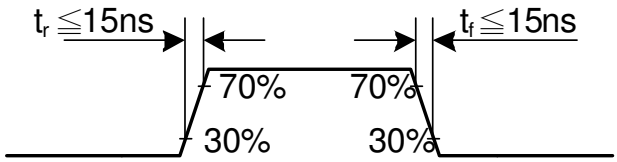
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

18.3.3. Display Serial Interface Timing Characteristics (3-line SPI system)

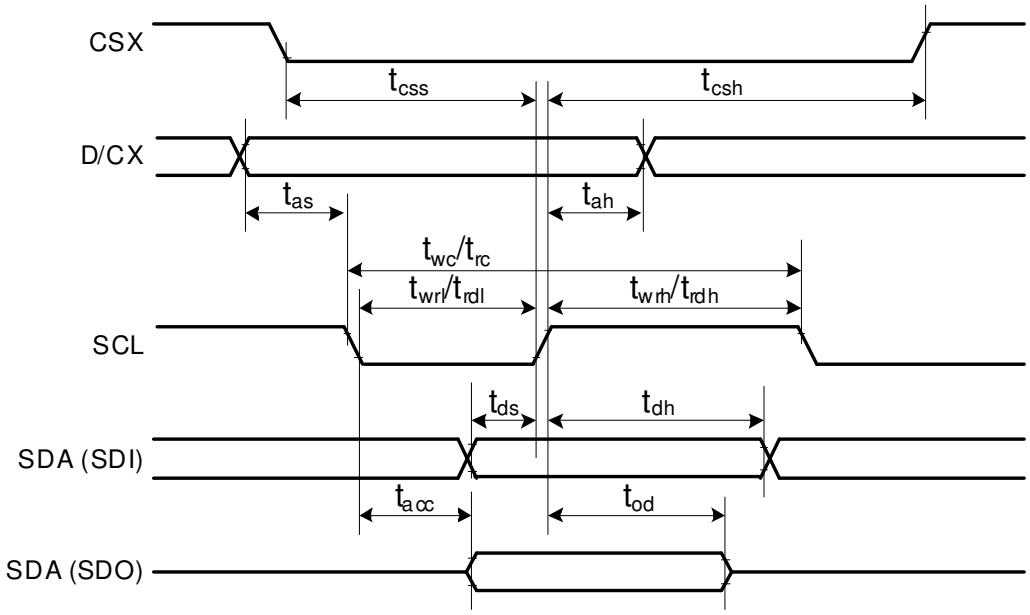


Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	66	-	ns	
	tshw	SCL “H” Pulse Width (Write)	33	-	ns	
	tslw	SCL “L” Pulse Width (Write)	33	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL “H” Pulse Width (Read)	75	-	ns	
	tslr	SCL “L” Pulse Width (Read)	75	-	ns	
SDA / SDI (Input)	tsds	Data setup time (Write)	30	-	ns	
	tsdh	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	-	ns	
	toh	Output disable time (Read)	10	70	ns	
CSX	tscc	SCL-CSX	20	-	ns	
	tchw	CSX “H” Pulse Width	40	-	ns	
	tcss	CSX-SCL Time(write)	15	-	ns	
	tcsh		15	-	ns	

Note: Ta = 25 ℃, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V

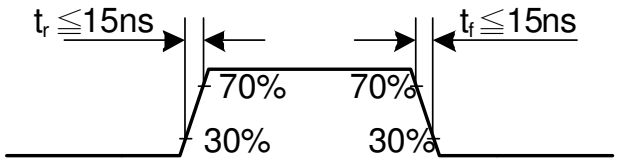


18.3.4. Display Serial Interface Timing Characteristics (4-line SPI system)

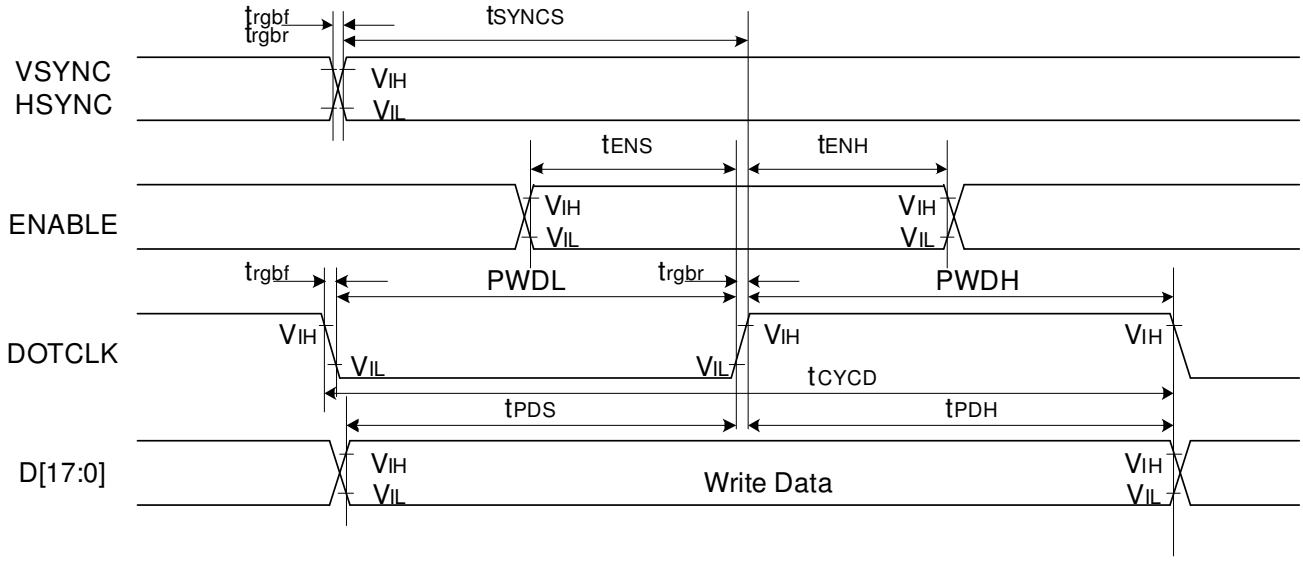


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	15	-	ns	
	tcsh	Chip select hold time (write)	15	-	ns	
SCL	twc	Serial clock cycle (Write)	66	-	ns	
	twrh	SCL “H” pulse width (Write)	33	-	ns	
	twrl	SCL “L” pulse width (Write)	33	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL “H” pulse width (Read)	75	-	ns	
	trdl	SCL “L” pulse width (Read)	75	-	ns	
D/CX	tas	D/CX setup time	10	-		
	tah	D/CX hold time (Write / Read)	10	-		
SDA / SDI (Input)	tds	Data setup time (Write)	30	-	ns	
	tdh	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	-	ns	For maximum CL=30pF
	tod	Output disable time (Read)	10	70	ns	For minimum CL=8pF

Note: Ta = 25 ℃, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V

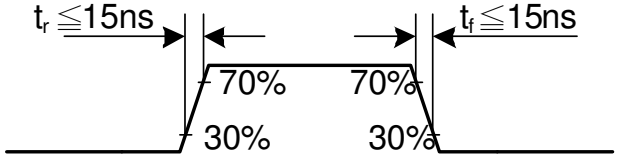


18.3.5. Parallel 18/16/6-bit RGB Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
D[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	33	-	ns	
	PWDL	DOTCLK low-level period	33	-	ns	
	t_{CYCD}	DOTCLK cycle time(18 bit)	66	-	ns	
		DOTCLK cycle time(6/6/6 bit)	50		ns	
	t_{rgbr} , t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	6-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
D[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level pulse period	25	-	ns	
	PWDL	DOTCLK low-level pulse period	25	-	ns	
	t_{CYCD}	DOTCLK cycle time	50	-	ns	
	t_{rgbr} , t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: Ta = -30 to 70 ℃, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V



19. Revision History

Version No.	Date	Page	Description
V0.01	2009/08/25	All	New Created
V0.02	2009/10/13	61,64	Serial Interface unused D[17:0] connect to GND.
		217	Add Configuration of Power Supply Circuit
	2009/11/09	175	Modify SAP Register
		All	Modify the IM pin interface definition
V0.03	2009/12/22	220 11	Modify external elements connected to the power supply circuit Modify the IM[3:0] for i80 Type II definition
V0.04	2010/01/11	6 221	Modify VDDI_LED description. Add voltage generation table
V0.05	2010/02/22	179	Remove AVDD = 3*VCI1 setting
V0.06	2010/3/25	226~233	AC/DC timing revise
		165	B6h description
V0.07	2010/03/30	101	Modify Sleep out restriction
V0.08	2010/4/19	191	ID4 description
V.0.09	2010/4/26	168,224	DSTB remove
V0.10	2010/4/30	191	ID4 description
V0.11	2010/6/09	86/168 232	DSTB description remove Add RGB 6/6/6 write cycle limitation
V0.12	2010/06/21	46/163	Add HBP restriction in by pass mode
V0.13	2010/07/26	216~218	Add Gamma voltage generation and Gamma correction formula
V0.14	2010/09/17	192~193 196 213 215~216	Modify E0h/E1h description Add F2h description Add VCI in the “Only the MCU interface and memory works with VDDI and VCI power supply” description. Add power/display on/off and sleep in/out sequence.
V0.15	2010/12/02	181	C2h description
V0.16	2011/02/25	231	Add STB current
V0.17	2011/03/03	231	Add STB current